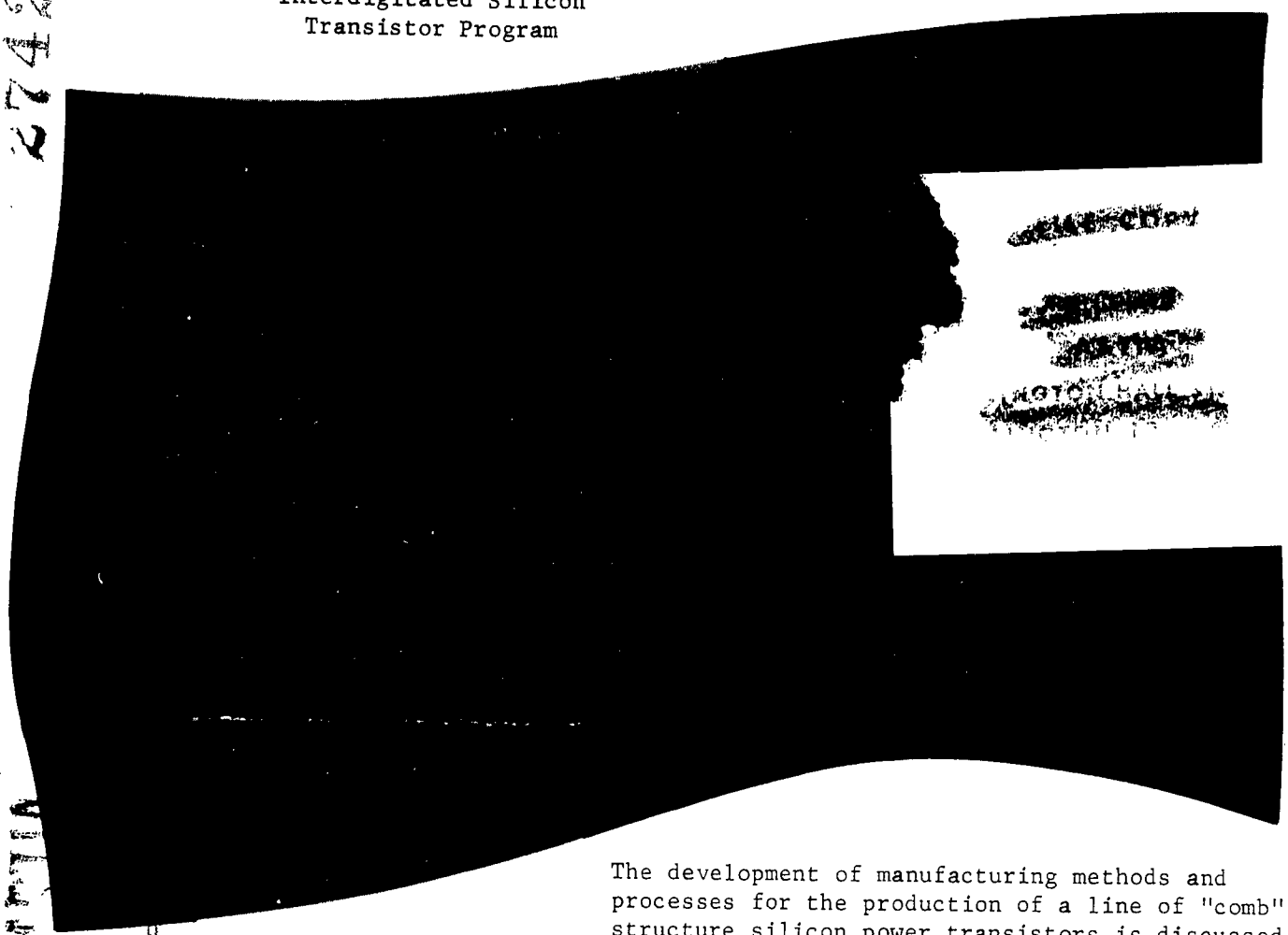
ASD TR 7-850(I)

ASD Interim Report 7-850(I)

January, 1962

Interdigitated Silicon Transistor Program



Electronics Branch

Manufacturing Technology Laboratory

Aeronautical Systems Division

United States Air Force

Wright-Patterson Air Force Base, Ohio

The development of manufacturing methods and processes for the production of a line of "comb" structure silicon power transistors is discussed. Analysis of the sequence of operations indicate the desirability of investigating a planar design using epitaxial techniques for collector deposition. Problems of doping and resistivity uniformity require extensive study. Diffusion, etching and assembly operations were studied with a view to improving fabrication techniques. Twenty ampere transistor design parameters are described.

Pacific Semiconductors, Inc.

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Abstract-Summary

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S. H. Barnes

B. Rappaport

F. J. Steinebrey

The development of manufacturing methods and processes for the production of a line of "comb" structure silicon power transistors is discussed. Analysis of the sequence of operations indicate the desirability of investigating a planar design using epitaxial techniques for collector deposition. Problems of doping and resistivity uniformity require extensive study. Diffusion, etching and assembly operations were studied with a view to improving fabrication techniques. Twenty ampere transistor design parameters are described.

Consideration of the possibility of replacement of the present collector contact diffusion process with an epitaxial process is deemed advisable since the latter will permit closer control of the collector contact thickness. The method employed is the thermal decomposition of trichlorosilane and deposition of silicon on a silicon substrate of low resistivity. Trichlorosilane was chosen because of its ease of decomposition in a hydrogen stream and its availability in reasonably pure form. The required resistivity of the deposited layer is eight ohm-centimeters. To meet this requirement, further purification of the trichlorosilane is necessary, and progress has been made toward this end.

Methods for increasing the capacity of the base diffusion process have been studied. The desirability of a vapor deposition method of supplying boron instead of the present boron oxide doped quartz flat source is indicated. Improvements in emitter diffusion techniques are also described.

A photoresist alignment jig for increasing the rate of the mask alignment operations has been designed.

The 3-20 transistor design was completed. Package design studies for all transistor types are under way.

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Interdigitated Silicon Transistor Program

S. H. Barnes
B. Rappaport
F. J. Steinebrey

Pacific Semiconductors, Inc.
Contract AF 33(600)-43029
ASD Project 7-850

Interim Technical Engineering Report
18 September 1961 - 18 December 1961

The development of manufacturing methods and processes for the production of a line of "comb" structure silicon power transistors is discussed. Analysis of the sequence of operations indicate the desirability of investigating a planar design using epitaxial techniques for collector deposition. Problems of doping and resistivity uniformity require extensive study. Diffusion, etching and assembly operations were studied with a view to improving fabrication techniques. Twenty ampere transistor design parameters are described.

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FOREWORD

This Interim Technical Progress Report covers the work performed under contract AF 33(600)-43029 from 18 September 1961 to 18 December 1961. It is published for technical information only and does not necessarily represent the recommendations, conclusions, or approval of the Air Force.

The contract was initiated under ASD project 7-850 and is administered under the direction of P.P. Poliquin, ASRCTE of the Basic Industry Branch, Manufacturing Methods Division, Aeronautical Systems Divisions, Wright-Patterson Air Force Base, Ohio.

The entire program is under the direction of S. H. Barnes, Manager of the PSI Transistor Division Engineering Department. Others who supervised various portions of the program are:

Administration and Planning	-	B. Rappaport
Device Development	-	F. J. Steinebrey
Device Engineering	-	L. Ornik
Product Engineering and Pilot Production	-	M. Doser
Package Engineering	-	B. Gray
Industrial Engineering	-	P. Loose

In addition to those listed above, the following professional personnel were actively engaged in the development work and in the preparation of this report:

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	A. Stein

This report has been given the PSI internal number 3000:37-1-Q.

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CHAPTER 1

Introduction

The objective of this program is to develop manufacturing methods, processes, and techniques for quality-quantity production of a family of interdigitated or "comb" structure silicon power transistors. The developed methods, processes, and techniques are to be demonstrated by fabrication of samples and the operation of an unbalanced pilot production line. The entire sequence of operations required to fabricate the required family of transistors has been analyzed and the points requiring additional process development have been determined.

Based on this study, the major process developments to be undertaken were determined to be the following:

1. Investigation of substitution of the epitaxial collector process in place of the present collector contact diffusion process. The major objectives are better process control, better device characteristics, reduction in number and complexity of processing steps, and faster manufacture by elimination of the one week collector contact diffusion step.

2. Substitution of the planar or isolated base structure for the mesa etch process. The principal objectives are better device characteristics, avoidance of re-

jects caused by misaligned wax ruling and failure of masking in acid etching, reduction in number and complexity of processing steps, and decrease in required hand labor.

3. Elimination or improvement of the dice etch process, possibly by a diamond scribe and break or a photoresist mask and etch procedure. The objectives are to reduce rejects caused by misaligned wax ruling and failure of masking during acid etching, a reduction in number and complexity of processing steps, and a decrease in required hand labor.

4. Plating build-up improvement of the base and emitter metallized regions. The major objectives are to eliminate rejects due to poor plating, improve device reliability, and reduce rework by more precise process control. New methods might be required.

5. Improvement of active region metallizing. Objectives are to substitute a new metallizing process or to improve the present modified electroless nickel method. At present, difficulties due to variation of operator technique and to surface contamination cause periodic increases in rejects and extra labor for rework.

6. Mount and lead attachment improvement. The main objective is to reduce rejects. It is desirable but not essential to increase the mounting solder melting temperature from 220°C to 300°C for better device reliability.

7. Improvement of photoresist processes. Objectives are to reduce labor and improve accuracy of alignment of wafers.

8. Improvement of acid etching of wafers to precise thickness. The major objectives are to reduce labor and to eliminate the wax mounting procedure. Wax mounting residues are known to adversely affect subsequent diffusion operations and epitaxial layer deposition with deleterious effects on yield and device quality.

9. Base predeposition. The main objectives are to eliminate the periodic rejects which result from specks of boron oxide contaminating the wafer surface in the present process and also to remove the small batch size "bottleneck" which prevents rapid mass production in this step.

10. Base redistribution improvement. No major problem exists in this area; however, improvements of the

base predeposition process may require some additional process work. Some improvement in accuracy of base depth control and in control of base oxide mask formation is desirable.

11. Emitter diffusion improvements. The major problems are lack of precise process control, formation of microscopic shorted spots on some of the potential transistors due to phosphorus pentoxide fog droplets and excessive labor in cleaning messy phosphorus pentoxide deposits from the equipment.

12. Miscellaneous process problems. Minor improvements are needed in such areas as protective surface coating, surface cleaning methods, improvement of lead attachment, improvement of lead bonding to electrodes, etc.

Complete solutions to all of the above suggested tasks will not be possible in the limited time allotted for process development work. However, areas having the most serious effect on device fabrication and quality will receive the most attention. Also, development tasks which are expected to take the longest time to complete are being started first. Some problems are expected to be solved during the normal course of operation of the present production line for ten-ampere power transistors and, hence, will cease to be problems for this program.

One of the considerations of this program is the physical design of the transistor so that, as far as is practical, the least number of packages could be used for all devices. Preliminary studies indicate the feasibility of limiting the number of packages to four - a single ended package for the 1-1 device (possibly a TO-8 configuration), a combined 2-10/3-20 package and both a water cooled and an air cooled combined 4-50/5-100 package.

In Chapter 2 we will first discuss the epitaxial collector process development effort. Some theoretical background will be given. Work on purification of materials and process techniques will be described. Next, the problem and preliminary results of resistivity control work will be covered. The preparation of starting wafers for epitaxial deposition will be described and, finally, the methods and results of operation of a prototype pilot epitaxial plant will be covered. Additional process development in the areas of base predeposition and redistribution, emitter diffusion, photoresist alignment improvement, and design of the twenty-ampere transistor structure will be found in the latter part of this chapter.

Chapter 3 will discuss briefly the status of package development for this program. Chapters 4 and 5 will outline the conclusions and the program for the next period.

CHAPTER 2

Process Development Work

2.1 Epitaxial Process Development

The major effort during the past period was devoted to a study of the epitaxial process in order to provide information upon which a subsequent decision may be made as to the advisability of replacing the present collector contact diffusion method with an epitaxial technique.

2.1.1 Because of problems inherent in the present collector-contact diffusion process, methods of improvement were felt to be imperative. The proposed improvement is to employ the vapor deposition or epitaxial technique for forming the collector region on a highly-doped (N^+) substrate. One of the principal reasons why an epitaxial collector process would be expected to be better is that it will enable direct control of collector thickness, whereas in the collector-contact diffusion process, the collector thickness is the difference between two measurements, one of which (the N^+ diffusion depth) is not presently capable of accurate direct measurement. While it is possible to correct for diffusion variability by control of the final thickness in etching, this last step is itself hard to control. Hence, the

resultant collector region thickness cannot be as closely controlled as is desirable for a high quality device with a high yield. Other problems with the present collector-contact diffusion method are staining of the wafers due to the large quantities of phosporus pentoxide employed, contamination in subsequent steps due to unremoved specks of phosphorus remaining on the wafer, high labor cost, and the yield loss attendant on running several processes consecutively. The substitution of an epitaxial collector process should reduce or eliminate most of these difficulties.

Briefly, the epitaxial process as practiced at Pacific Semiconductors consists of the thermal decomposition of either trichlorosilane or silicon tetrachloride with the deposition of oriented silicon on a monocrystalline silicon substrate of low resistivity, thus producing a layer of silicon of higher resistivity which continues the original silicon lattice. At the present time, the problems of layer thickness and monocrystallinity have been solved, but the problems of doping and resistivity uniformity still require extensive work.

In this section, we will discuss the theory involved in the epitaxial process, possible methods of purification of trichlorosilane and silicon tetrachloride, various techniques which have been used in the deposition process and reasons for their acceptance or rejection, present and proposed methods of adjusting the resistivity to a suitable level, preparation of substrate wafers for the deposition, and finally a description, the results, and the problems encountered in a prototype pilot line. A number of proposed methods have been tried and accepted or rejected on practical or theoretical grounds. Other methods are now being evaluated or will be evaluated in the near future. A brief summary will conclude this section.

2.1.2 Theoretical Discussion

Until fairly recently, the preparation of single crystal semiconductor materials by methods other than solidification from the liquid phase had not been extensively investigated. There were various techniques of vaporizing a substance and subsequently depositing it unaltered upon a desired substrate. These methods are well known and have been widely practiced in basic research and, more recently, have been extended to the commercial and industrial applications of thin films. Such vapor deposited layers, whether in vacuum or inert atmosphere, are

usually polycrystalline. There is evidence, however, that even such deposits tend to grow in preferred orientations.[1] This orientation originates from the tendency of atoms, ions, or molecules to aggregate in close packing to form plane sheets of monoatomic or monomolecular thickness on the substrate. This is particularly so when their mobility on the substrate is high at the condensation temperature. However, this is only a tendency, and special conditions need to be met if one wishes to consistently produce a single crystal deposit of any magnitude and of good crystallographic perfection. This is important for the manufacturer of devices from epitaxial silicon layers, since the capability of a semiconductor device is affected by the crystal perfection of the structure.

Now it is a reasonable assumption that one would be more likely to get a single crystal deposit from the gaseous phase if the substrate used was a single crystal of the same material. In effect, one provides a "ready-made" pattern for the condensation of the vapor. This is the basis for the vapor-deposition epitaxial process. Epitaxy is defined as the "oriented intergrowth between two solid phases. The surface of one crystal provides, through its structure, preferred posi-

tions for the deposition of the second crystal."[2] The usual epitaxial situation involves two phases of the same material. This, however, is an arbitrary restriction and true epitaxial deposits are also possible between different materials if there is some sort of periodic match between the lattice constants of a crystal substrate and the deposited crystal structure.

Crystal growth phenomena are extremely complex, and there is at present no detailed comprehensive theory. Fortunately, the general mechanism of growth from the vapor state is fairly well understood, and we will now attempt a simplified explanation, as certain aspects seem to apply to the epitaxial deposition of silicon. A more detailed treatment can be found in the literature.[3,4,5,6]

At this point we need to distinguish between an ideal crystal and a real crystal. The first is structurally perfect; every atom is properly surrounded by neighboring atoms, the only permitted perturbations are elastic strains or thermal vibrations that leave the crystal structure unchanged. A real crystal will almost invariably be subject to some structural defect. This distinction is made because, historically, the study and under-

standing of crystal growth actually developed this way. W. Gibbs (1878) gave the first general theory based on thermodynamics. Continued efforts, including the development of an atomic theory of growth in the last 35 years led to predictions that contradicted experiment. A re-examination of some aspects of the previous theories, particularly by Burton, Cabrera, and Frank,[7,8] brought the recognition that real crystals in nature are not perfect. They introduced a theory taking the imperfections into account, were able to remove the above-mentioned contradictions, and predicted the form of growth surfaces which were later observed.

Growth of a Perfect Crystal

To illustrate the growth process we use the Kossel (1927-1928) model. The atoms (molecules or ions) making up the crystal are considered as cubes. The entire crystal is built by sta ing cubes face to face. It is assumed that each cube is attracted equally by all its six neighbors, and the only interaction is between nearest neighbors. This structure is illustrated in Fig. 1 and may be assumed to be a crystal in contact with its vapor. The cube is used only for sake of simplicity. One incomplete layer and nucleated area are shown in the figure. The boundary line where there is a difference in level equal to the effective atomic diameter is called a "step" on

the surface. In general, the step will be incomplete and will have "kinks" or re-entrant corners of the types marked B and D. Atoms from the vapor are absorbed on the surface, A. Theory indicates that such an atom diffuses so rapidly on the surface that it effectively travels many lattice distances before re-evaporating. If the atom hits a step, say at C, as it moves over the surface, it will tend to be more tightly bound than at A, since it now has two nearest neighbors instead of one. The atom will now tend to diffuse along the step. If it now reaches a kink, D, it will be even more tightly bound since it is now in contact with three neighbors. At any given temperature there will also be a tendency for the atoms to return to the vapor state. The frequency of joining and leaving the kinks will be equal if vapor equilibrium is attained.

Suppose now, that by some means, the vapor pressure is increased over the equilibrium value. Since rate of arrival of atoms is proportional to vapor pressure and rate of evaporation depends on temperature, there will be more atoms being bound to the re-entrant points than leave, and as a result the step will grow. This growth will continue as atoms are added to the step and will stop only when the layer is complete and has reached the edge of the crystal face.

For further growth it now becomes necessary to have a nucleus of atoms (shown at E, Fig. 1) on the completed face. We are considering here a homogeneous nucleation, that is, no other phase or impurity atoms are involved. In the case of a perfect crystal, it is the ease of this nucleation that limits the rate of growth. The problem is similar to the problem of nucleating a water droplet. It has been shown that the probability of formation of nuclei is a very sensitive function of supersaturation and is quite unlikely below a certain critical value which may be from 25 to 40% supersaturated, depending upon typical values of the constants involved. We may assume then, that depending upon the degree of supersaturation, atoms from the vapor will collide with the crystal and some will effectively condense on the surface, giving up their latent heat and thereby tending to increase the surface temperature and the mobility of atoms on the surface. Clusters of atoms will tend to form, since the condensing atoms will prefer sites with a maximum number of nearest neighbors. And, just as there is associated with the surface energy of a water droplet a local equilibrium vapor pressure that increases with the curvature of the droplet, there will be associated with the energy of these atom clusters on the crystal face a local vapor pressure inversely proportional to

the radius of curvature of the exposed surface. Assuming these clusters will be round, a nucleus with a small radius of curvature has a high equilibrium vapor pressure. For such a nucleus, the supersaturation, being the excess of the ambient vapor pressure over the local equilibrium pressure, is less than for a nucleus of larger radius. If the nucleus is small enough, the supersaturation may be negative, and the nucleus will evaporate, leaving the larger clusters to provide a foundation for the lateral growth of that particular layer. Growth will continue until the "islands" again grow out to the extremities of the surface. At this point more nuclei must be formed for further growth. This will be no problem, if the supersaturation is above the critical value, and growth will not be limited by nucleation. In fact, the rate of growth will increase rapidly with supersaturation.

A basic difficulty arises because, in general, it is found that, for those crystals which grow, the growth rate is proportional to supersaturation down to values much lower (3 to 4%) than the critical supersaturation as calculated from the surface nucleation theory. In fact, the growth rates obtained in practice are just what would be expected if nucleation of atomic clusters did not occur and the condensing atoms found steps always present on the surface. It was this that led to the postulation of real imperfect crystals.[7,8,9]

Growth of an Imperfect Crystal

The type of flaw of primary importance in this growth problem is a geometrical fault called a screw dislocation. The concept was first introduced by Burgers (1939) and may again be illustrated by a crystal model using a simple cubic structure (Fig. 2). Consider a cut, ABCD, in the crystal with the material to the right of the cut pushed down by one atomic diameter. A partial step has now been created on the surface. The dislocation line CD is the boundary line between the slipped and the perfect parts of the crystal. The crystal structure is essentially perfect up to a few atomic distances away from the dislocation line, but near the line some irregularity will exist.

Looking at Fig. 3 it is obvious that atoms condensing on the crystal surface and diffusing to the step of the dislocation will cause that step to advance. The situation is now different from the advance of a step on a perfect crystal in that it is now impossible for captured atoms to produce a complete atomic layer. The surface is now in the form of a spiral ramp. The step can never be eliminated for, since the end of the dislocation remains fixed, new atoms have the effect of rotating the step around the fixed point. Since for a given supersaturation each point on a straight step will advance with the same speed, that part of the step near the dislocation will have

a higher angular velocity and advance through a larger angle in a given time than those parts of the step further out. This greater angular advance has the effect of increasing the radius of curvature of those parts of the step. This will increase the local equilibrium vapor pressure and, since the rate of advance of a section of a step is proportional to the excess of vapor pressure over the local equilibrium vapor pressure, those parts close to the dislocation line will now tend to advance more slowly than the outer parts of the dislocation. A steady state will finally be reached in which the angular velocity will be the same for all points on the step. In the steady state the whole spiral will rotate uniformly about the dislocation line as the surface continues to grow. The validity of this concept of low supersaturation growth has been well verified by many observations of the above-mentioned spirals.

The Epitaxial Problem for Silicon

From the above discussion it would seem that there should be no problem at all in growing single crystal material from the vapor phase. We require a clean, properly oriented substrate of silicon single crystal; a properly-designed, easily-maintained, contamination-free, non-oxidizing deposition chamber; a source of silicon vapor;

and the means of transporting this vapor to the desired substrate. A sufficiently high supersturation level of the silicon vapor relative to the equilibrium vapor pressure of the substrate would provide all necessary nucleation. A substrate temperature adequate to produce high mobility of the silicon atoms on the surface would insure growth. Once the basic information on process conditions and techniques is collected and understood, an extension to full-scale production should follow.

Unfortunately, there are some serious problems involved here. Consider the question of producing a proper concentration of silicon vapor. The obvious approach is to use an evaporation technique. However, it is difficult to evaporate oxide-free films of silicon.[1] The source temperature required is rather high, but the substrate temperature required could be about the same as for vapor deposition. The deposition rates, however, are generally considerably slower than for vapor deposition.[10] There are other inherent difficulties in this procedure which will not be discussed here. The technique, widely investigated today, is to employ some sort of gas phase reduction. In this method a gaseous compound of silicon is brought into close contact with a heated silicon substrate. The compound is reduced to elemental silicon either

by heat or a combination of heat and a reducing agent, such as hydrogen gas. Thus, a high density of silicon atoms will be produced on or adjacent to the heated substrate, and the basic mechanism for crystal growth, as described previously, should operate. It must be remembered that this physical and chemical situation, so briefly stated, is quite complex, being probably a heterogeneous type of reaction. A reaction occurring at a surface may be separated into a number of steps, the slowest of which will be the rate-determining step for the overall process.

1. Transport of gaseous reactants to the surface.
2. Adsorption of gases on the surface.
3. Desorption from the surface.
4. Surface reactions.
5. Transport of liberated products from the surface into the gas phase.

The determination of the relative importance of various steps in any vapor deposition process involves a detailed study of the reaction kinetics, and is beyond the scope of this study. However, if step 1 or step 2 is the rate-determining step the process would be diffusion limited and the temperature coefficient for the rate would follow a square root relationship. The energy of activation, ΔE, for surface reactions is generally high ($\sim$30 Kcal/mole), whereas ΔE for diffusion processes is smaller. As work

continues in this field, more exact knowledge of the mechanism will be developed.

From the previous discussion we might conclude that more reliance must be placed on empirical rather than exact scientific knowledge in developing an epitaxial process. We can state certain general principles, however. For example, the mechanism is such that a dislocation will tend to propagate. Consequently, the substrate material should be of low dislocation material in order to grow the desired low dislocation region. Also, substrate temperature must be high enough to give adequate surface mobility, otherwise epitaxy will not occur as atoms will not be free to move around and find a proper site on the crystal lattice. The vapor phase must be supersaturated with respect to the vapor pressure of atoms on the surface, otherwise deposition cannot take place or the surface might actually become etched. Finally, we must conclude that with the high surface mobility essential to epitaxial growth, we will of necessity experience difficulty with impurity atoms in the substrate migrating into the newly deposited layer with a consequent adverse effect on layer composition. Indeed, some of the substrate impurity atoms will be picked up in the gas phase and redeposited on considerable distance away from their original site.

Selection of Silicon Compound for Vapor Growth

All of the halides and substituted halides of silicon would seem to be potentially applicable to our requirements. However, an analysis of thermodynamic date for the reduction of these various compounds combined with considerations of availability, purity, and operational difficulties narrows the choice considerably. Examining the free energy change as a function of temperature can provide useful information about a possible chemical or physical change. Theoretically, a process can occur spontaneously, if it is accompanied by a decrease in free energy.

The free energy versus temperature curves are presented in Fig. 4 and Fig. 5. From Fig. 4 we see that only for silicon tetraiodide and silane does the free energy go to zero below the melting point of silicon (1430°C). Theoretically, we should be able to use these compounds for vapor phase growth by direct decomposition. Controlled introduction of silicon tetraiodide into a reaction chamber would cause some difficulty, as it is a solid at room temperature and has a narrow liquidus range. Silane decomposes essentially irreversibly, and therefore, the removal of silicon atoms not deposited on the proper lattice sites would be less likely. If we use hydrogen as a reducing agent, Fig. 5 shows that at least three other materials should be useable.

Silicon tetrabromide is not commercially available in the required purity. Trichlorosilane and silicon tetrachloride are similar in physical properties and can be expected to react similarly with hydrogen. The curve shows that trichlorosilane should be reduced to the element at about 1050°K. This is about 300°C below the decomposition temperature of silicon tetrachloride. Lower temperatures on the substrate are an advantage in maintaining a minimum of impurity diffusion. Also, the reduction of silicon tetrachloride probably proceeds through trichlorosilane as an intermediate. Consequently, it was decided to employ trichlorosilane in the epitaxial work.

The reaction of interest might be written as:

$$HSiCl_3\ (g) + H_2\ (g) \longrightarrow Si \downarrow + 3HCl\ (g)$$

However, the true mechanism is probably not this simple. Also, in addition to collisions with hydrogen, the trichlorosilane may react with itself or with the reaction products and intermediates.

All systems employing trichlorosilane must exclude air (oxygen) and water vapor. Oxygen forms a barrier film on the silicon, thus preventing proper deposition, while vapor will either oxidize the silicon or react with the trichlorosilane to form silicon monoxide or oxyhydride

which also deposits on the wafer with possible harmful results. Slight traces tend to deposit on the reaction chamber walls and, while they may not be particularly harmful, they require frequent cleaning of the vessel.

Fig. 6 is a schematic illustration of the basic equipment used for experimental work on vapor reduction of trichlorosilane. Pure hydrogen is provided by first passing commercial dry hydrogen through a "Deoxo Puridryer" unit to remove slight traces of oxygen and moisture and then through two liquid nitrogen cold traps for additional drying. The purified hydrogen may now go directly into the reaction chamber or be bubbled through the trichlorosilane. In many experiments the trichlorosilane was maintained at -77°C by immersion in a dry ice and acetone bath. When varying vapor pressures of trichlorosilane are wanted, the source is placed in an insulated chamber that can be cooled or heated over a wide range. A plot of the experimental trichlorosilane pick-up rate as a function of the hydrogen flow rate is depicted in Fig. 7. The theoretical curve was derived as follows:

We assume the ideal gas law, $n = \frac{PV}{RT}$

V is the volume of the system represented by the hydrogen flow rate (cm^3/sec) plus the volume of trichlorosilane vapor picked up by the hydrogen. It is assumed

that the evaporation rate is rapid enough to maintain the equilibrium vapor pressure.

The bubbler trap temperature determines the trichlorosilane vapor pressure; hence, the value of P/RT is a constant, K, dependent only on bubbler temperature. Substituting in the ideal gas equation, we have $n = KV$, where $K = P/RT$. The weight of trichlorosilane is n times the molecular weight. The experimental curve approaches the theoretical line at low flow rates as expected. To obtain reproducible concentrations with a bubbler trap, attention must be paid to the following sources of trouble: trichlorosilane level and coolant level of bubbler, flow rate of hydrogen, temperature control, and heat transfer rate between the coolant and the trichlorosilane.

The substrate heater in the reaction chamber is a cylinder of graphite (AUC grade). A 2.5 kw RT generator drives a coil on the outside of the reaction chamber. The work coil is mounted so that it may be moved to an optimum coupling position for heating the silicon slice. Temperatures are measured with an optical pyrometer and controlled by varying the generator output current. The hydrogen and trichlorosilane mixture passes vertically down over the clean silicon surface, depositing silicon wherever a sufficient temperature exists. Not all of the trichlorosilane in the mixture will be reduced. In terms

of the material actually converted to epitaxial silicon, the efficiency of the experimental equipment is generally 15 to 20%. Variations are primarily a function of the geometry within the reaction chamber and of the resultant flow patterns. The gas, exhausted to a fume hood or absorption trap, will normally contain some unreacted trichlorosilane, hydrogen chloride, intermediate chlorosilanes, and polymers.

It has been found that the preparation of the substrate surface is important for good single crystal growth. There is usually enough native oxide even on a freshly etched surface to cause some difficulty. The wafer is heated in hydrogen at 1200°C for 10 minutes prior to turning on the trichlorosilane. This treatment removes the oxide layer which evaporates apparently as silicon monoxide and condenses on the cold walls of the reaction chamber.

Reproducible single crystal deposits of silicon have been obtained using a substrate temperature ranging from 950° to 1150°C at hydrogen flow rates from 1 to 5 cfh. Depending upon the area of the substrate geometry, gas flow rate, and other variables, a deposition rate of from 25 to 40 microns per hour is easily obtained. Fig. 8 shows curves of the experimentally determined deposition rates of silicon versus the partial pressure of trichlorosilane

for various substrate temperatures. It indicates a non-linear behavior with increasing concentration of trichlorosilane in hydrogen. This non-linear behavior is not presently understood but it should be clarified by additional reaction kinetics studies. It is interesting that if we assume the rate of deposition (Rd) follows an exponential law of form:

$$Rd = Ae^{\frac{-\Delta E}{RT}}$$

A = constant
E = activation energy

$$\text{then} \quad \ln Rd = \ln A \frac{-\Delta E}{RT}$$

and, plotting ln Rd versus 1/T should give a straight line having a slope equal to ΔE. Fig. 9 is such a graph for trichlorosilane at one partial pressure. Other partial pressures will give parallel lines. From this line we find ΔE is equal to 25.5 kilocalories per mole. This is a rather large value. It must be emphasized that this is the activation energy for deposition and not necessarily the energy for the reaction. If the process is kinetically limited by the surface reaction, the activation energy could be expected to be high and possibly not too different from this value.

Under normal operating conditions the process generally yields n-type single crystal deposits ranging in resistivity from 0.5 to 3 ohm-cm. The resistivity is in part determined by contamination during storage and bottling. A more con-

sistent effect on resistivity is that produced by a low resistivity substrate. At the usual operating temperatures, chemical attack of the ambient atmosphere on the substrate produces enough volatile compounds to drastically affect the "doping" level of the epitaxial layer. Fig. 10 is a series of experimental curves showing how the resistivity of n-type deposits increased with decreasing resistivity of p-type substrates and increasing substrate temperature.

Some general references on epitaxial work are listed at the end of the bibliography.

2.1.3 Purification Studies

In the proposed use of epitaxy for the collector region of the required high-power transistors, precise control of resistivity is essential. The 8 to 12 ohm centimeter range presently believed essential to meet collector voltage requirement cannot now be provided with any degree of uniformity. A significant cause of variation in the resistivity of the deposited silicon can be traced to impurity of the trichlorosilane used as a source of vapor. Obviously, if there is to be any hope of dopant control this variation in the source material must be removed or reduced to a minimum. The suppliers are aware of the problem and have traced

much of the trouble to the difficulty of handling and storing small quantities (small surface-to-volume ratio) of this highly reactive material. They expect that this problem will be adequately solved in the near future with the development of special pressurized containers and associated valving. Since much of the contamination occurs after the material leaves the suppliers, it would seem advisable that purification techniques be developed for use on the epitaxial line so that a source of highest purity is available.

The first approach taken was a duplication of the silicon tetrachloride purification reported by H. C. Theuerer [11] of Bell Laboratories. This is an adsorption technique using columns of various materials. Theuerer reported using silica gel, activated alumina, charcoal, and various "molecular sieves" and claimed best results with silica gel and activated alumina. Using a relatively simple column with trichlorosilane, we experienced great difficulty because of the ease with which trichlorosilane picks up moisture. A redesigned column was built which could be pumped out completely and which would allow separation of the various fractions coming from the column without opening the system and possibly introducting contamination and moisture. Fig. 11 is a drawing of the new equipment. The

first trials using silica gel (6-16 mesh) activated at 270°C for about twenty hours gave no noticeable improvement on any of the three fractions. Work is continuing with this column. Other adsorbents are being tried. A major difficulty is achieving a thorough washing of the column materials prior to drying and activation.

2.1.4 Techniques

Enough information on potential sources of difficulty in the epitaxial process have now been accumulated so that certain observations and recommendations can be made. These should be taken into consideration in building future equipment for experimental or production purposes.

The Engelhard Industries "Deoxo Puridryer" seems to be adequate for removal of oxygen. However, cold traps are needed to insure complete removal of moisture. The present use of liquid nitrogen, dewar flasks and glass traps to remove the last trace of moisture is a nuisance and presents a potential breakage hazard. It is usually necessary to refill the dewar flasks several times during the course of a day's work. New traps made of coiled copper tubes immersed in dry ice and "Dowanol EE": (ethylene glycol ethyl ether) work quite well, and the

temperature (-77°C) is maintained all day without difficulty or attention. This whole complex of "Deoxo" unit and cold traps, however, should ultimately be replaced with a palladium diffusion tube hydrogen purifier for highest gas purity with greatest simplicity and ease of operation.

In general, any epitaxial equipment should be designed and built so that it can be easily taken apart for cleaning and yet, when assembled, maintain an air and moisture tight environment. It was found that ground connections of any type gave trouble because of contamination from the lubricant used for sealing. Problems were found with Kel-F, silicones, and other types. All such connections were replaced with a standard type of Pyrex seal with O-ring. These, used without any lubricant, proved very satisfactory. From a safety point of view, all breakable parts of the system should, whenever possible, be replaced by metal. The problem of making connections between metal and glass tubing was solved by using all Teflon unions, tees, etc. Glass stopcocks, for controlling gas flow, can be replaced by all Teflon on-off and needle valves.

The surface preparation of the silicon substrate requires a great deal of additional work. Microscopic examination

of the substrate prior to deposition is advisable. Often a surface which appears to the naked eye as a bright mirror will show under closer examination a great deal of chemical stain, wax residue, and even crystalline deposits. In addition, many surfaces show pitting. If any of these are present, the epitaxial layer will show defects at these places, and difficulty in later processing will generally result.

Using RT to produce the necessary temperature requires the presence of some type of susceptor in the reaction chamber. This becomes a source of possible adverse impurities. It is possible to use silicon itself as a susceptor, but the presence of some conductor is needed to provide initial coupling until the silicon is warm enough to couple to the RT field itself. Thus the contamination problem still remains, complicated by the difficulty of machining silicon for different geometries.

Much of our work has been done using high purity graphite as a susceptor. It machines easily and there is no coupling problem. Unfortunately, after a series of runs the graphite, being porous and absorbent for many gases, becomes contaminated. It then affects the doping of the epitaxial layer in an uncontrolled manner. This problem can be effectively overcome by using an inverted, long

quartz cup over the graphite, the silicon substrate now resting on the quartz cup. In this way, any material vaporizing out of the heated graphite tends to be carried down and out the exhaust with little chance of contaminating the silicon epitaxial layer.

2.1.5 Resistivity Control

In order to achieve the goals stated in the introduction of this chapter, that is the control of the resistivity and type of the epitaxial layer, it is necessary to add a dopant to the layer. This dopant may be added either to lower the resistivity, to raise it, or even to change conductivity type. In the epitaxial process practiced at Pacific Semiconductors, three methods seem possible. These methods are:

1. The direct addition of a doping agent to liquid trichlorosilane.
2. Direct Insertion of dopant vapor into the hydrogen-trichlorosilane stream.
3. Insertion of a hydrogen carrier gas containing a small amount of dopant into the main hydrogen-trichlorosilane stream.

In the method involving the direct addition of dopant to the liquid trichlorosilane, one of the major problems is the extremely small amount of dopant necessary. A specific example of the calculated amount necessary should prove instructive. The case involved a change from 2.4

ohm-cm P-type material through intrinsic to 0.7 ohm-cm N-type.

1. Carriers to be added ..... $2.2 \times 10^{16}/cm^3$

2. $\frac{P}{Si} = \frac{2.2 \times 10^{16}/cm^3}{4.96 \times 10^{22} \text{ atoms Si}/cm^3} = 4.4 \times 10^{-7}$

3. $\frac{\text{ml. } PCl_3}{\text{ml. } HSiCl_3} = \frac{1.34 \times 137 \times 4.4 \times 10^{-7}}{1.57 \times 135} = 3.8 \times 10^{-7}$

This implies that only 0.000038 ml of PCl_3 should be added to 100 ml of $HSiCl_3$. Because this small an amount is impractical to handle, successive dilutions had to be made. This is additionally difficult due to the necessity of handling the $HSiCl_3$ in an inert atmosphere box. The method was employed with reasonably successful results, although it was found that the amount of doping necessary was approximately four times higher than calculated. The discrepancy could have been caused by a fractional distillation effect and by a reaction rate difference in the deposition.

During these studies, it was also found that the dopant level in the $HSiCl_3$ changed with use and consequently caused a change in the resistivity of the deposit. This was ascribed to the fractional distillation commented on above. The major drawback to the method is, however, that the doping level or type can not easily be changed. It is necessary to have a separate injector for each type

and resistivity desired.

As a result of these difficulties, the second method was tried, direct insertion of the dopant vapor. A system similar to that used for the injection of trichlorosilane was used. After some initial difficulties, this second method seemed to yield reasonable reproducibility. The major difficulty encountered here was that the amount of vapor to be introduced was very much smaller than that of the trichlorosilane. This made the apparatus more difficult to build and required a skilled operator for reliable operation. It has the advantage that the doping level can be rather easily changed.

2.1.6 Preparation of Wafers for Deposition

All silicon wafers to be used as substrates for the epitaxial growth studies are put through a rigid input quality control procedure. In addition to certification by the vendor, mechanical and electrical tests are made and sample wafers are etched for dislocation studies. The vendor certifies that all wafers supplied are monocrystalline and of low dislocation material (less than 100 pits per square centimeter). They must also be of proper conductivity type, proper crystal orientation, proper thickness, proper resistivity, and correct diameter. The wafers

are assigned numbers by the vendor which indicate the ingot number and the order in which the slices were removed from the ingot. The inspection in our plant consists of a 100% sample inspection for correct diameter, thickness, and chips in the edge which would cause rejection. Spot checks are also carried out to verify the resistivity and dislocation count.

The accepted wafers are then subjected to a lapping procedure to reduce thickness, remove saw damage, and produce a parallel surface. At present, three methods are being used interchangeably, the choice of method being dictated by conditions existing at the particular time. The preferred method is the use of a planetary lapping machine which allows the simultaneous lapping of both sides and requires no mounting of the wafers. This machine will reduce ten of our wafers to final thickness in thirty to forty minutes. If difficulty is encountered from wafer breakage or it is desired to lap only one surface, the wafers are mounted on 0.25 inch thick solid carriers and lapped as above. With this system, the time required for thickness reduction is essentially doubled. The third method uses a 12 inch Crane Lapmaster. The wafers are mounted on three parallel lapping jigs and these are then placed in holders on the lapping plate.

The lapping vehicle is recovered for reuse by filtration to remove used abrasive and silicon, adjusted to proper viscosity with either water or Vehicle Concentrate.

When the wafers have reached the desired thickness, they are removed from the lapping machine and the vehicle is removed by a vigorous wash in distilled water. Wafers which have been mounted on jigs or carriers are then demounted and the wax removed with hot trichloroethylene. Wafers from all three methods are then cleaned ultrasonically. After this, they are placed in hot trichloroethylene, quenched with methanol, and rinsed in pure methanol. The wafers are stored in clean filter paper in envelopes until they are ready for etching to required thickness.

In order to produce a surface which is polished and free from work damage, the final thickness reduction is accomplished by means of chemical etching.

A serial number is assigned to each wafer completing the etching process, which is used to identify the wafer. The vendor's numbers are also retained for reference. Records are kept of all slices bought, wafers processed and wafers used during this contract.

2.1.7 Pilot Equipment and Operation

Before installation of the epitaxial processing developed in the production facility, it is almost essential to test it in a pilot operation. The pilot epitaxial deposition equipment is a scaled-up version of the developmental equipment mentioned previously. The reaction chamber is much larger. To achieve the same linear rate of flow of gases in the larger reaction chamber, the total system must also be constructed of larger tubing and related parts. The R.F. generator used to heat the pedestal in the reaction chamber is also larger to provide sufficient current to heat the larger mass of the pedestal uniformly and to the same operating temperature. There have been few changes to make the system easier to operate by the technicians, as compared to the developmental version.

The trichlorosilane is loaded into a quartz vessel in a dry box to prevent contamination and moisture pick up. For high resistivity deposits, specially pure material is required. Work on trichlorosilane purity is covered previously in this chapter.

2.1.7.1 Procedure for Deposition

The wafers for epitaxial deposition are processed as described under wafer preparation. They are now given a visual inspection for

imperfections and entered into the process chart and a run number is assigned. The wafers are stored in clean dry jars after post-etch washing and drying. Since the wafers are stock-piled before use, a small oxide layer will form which must be removed by a ten-minute wash in hydroflouric acid at room temperature.

The wafers are loaded onto the reactor pedestal which is stored in the dust-free box between runs. A minimum amount of time is used in transferring the pedestal from the dust-free box to the reaction chamber.

With the reaction chamber in place, a 20 minute purge of hydrogen is initiated to remove all air from the chamber before heating. When the purge is complete the R.F. generator is turned on and the wafers brought up to temperature for a final cleaning by thermal etch in hydrogen.

At the end of the thermal etch the temperature is changed to the deposition temperature and trichlorosilane is turned on for the desired length of time. After the deposition has taken

place, the trichlorosilane is turned off and a straight hydrogen purge is employed for five minutes to clear all traces of reaction by-products from the chamber. The R.F. can now be turned off and the wafers allowed to cool in hydrogen with reduced flow. When the pedestal is cool enough to handle, it is removed to the dust-free box. After a visual check, the wafers are replaced in the original clean jars to maintain identity.

In order to evaluate the N region on the N^+ substrate, a monitor wafer of P-type material is included in each run. The monitor is checked for sheet resistance with a standard four-point probe. Uniformity of sheet resistance is checked by measuring at the center and at four positions nearer the edge. To get a value of resistivity from the sheet resistance the thickness of the deposit must be known. The usual procedure is to angle lap a piece of the wafer and preferentially stain it with a suitable hydrofluoric acid staining etch. The depth is then found by counting interference fringes between the sample and an

optical flat under monochromatic light. A second method is to pot the slice on edge in a lucite block, lap the block down to the desired spot, preferentially etch the edge and then read the thickness directly under a microscope with a filar eyepiece. The uniformity of the deposition is checked by taking many readings across a sections of the wafer. As long as the wafers are uniform in area and deposition, a third method may be employed, namely, to compare the weight of the wafer before and after deposition by use of an analytical balance.

The required power transistors for this program should have collector regions of 8 to 13 ohm-centimeters resistivity and of 29 to 37 microns width before base diffusion. Early epitaxial experiments indicated that, while the thickness control could be rather easily met, resistivities in this range on low resistivity substrates were beyond the present process capabilities. Some of the difficulties can be seen by referring to earlier parts of this chapter. For example, the substrate resistivity which must be low to obtain maximum advantage

of the epitaxial process, causes impurities to be present in the reaction area. This results in the epitaxial layer becoming more "N"-type than is desired. Special geometries for the epitaxial reactor and high gas flow velocities reduce this effect. Also, the starting material is typically contaminated with "N"-type impurities. Purification methods and/or purer starting materials appear essential. Sources of contamination were found in the joint and stopcock sealants used in the apparatus, thus requiring development of equipment for their elimination. Finally, doping control has to be achieved. Direct addition to the trichlorosilane proved only partly successful to date and techniques were not readily adaptable to a production line operation.

Since resistivity control in the higher resistivity range is essential for employing the epitaxial collector process to the desired devices, these problems must be solved. However, so as not to delay solving other technical problems, it was determined to operate in a resistivity range where control was now satisfactory.

The operating point chosen for study was a collector region of 0.6 ohm-centimeters resistivity and 8.0 microns thickness. Evaluation included making actual devices from sample lots. All experiments were evaluated for deposited layer thickness and resistivity. Results of resistivity and thickness measurement for pilot runs are shown in Figures 12 and 13. Table I gives results of collector-base reverse voltage tests on transistors made from various epitaxial wafers. The voltages are approximately correct for this resistivity range.

2.1.7.2 Problems Encountered and Proposed Solutions

The largest problem at present is a variation in resistivity across the wafers. It was originally thought that this was due to a radial temperature gradient on the pedestal, but this problem was eliminated by redesigning the pedestal. The variation still exists. The geometry of the system and gas flow will be investigated as a remedy to this problem. We have had no trouble reproducing fairly low resistivity epitaxial deposits, but the available trichlorosilane is not pure enough to give high resisti-

TABLE I

Data on Epitaxial Wafers Submitted to the Transistor Plant

Wafer No.	Thickness (microns)	Collector Region Resistivity *	Average Voltage	Reverse Voltage at 100 μa
68-381	7.0	0.51	45	(28-60)
68-383			39	(17-60)
69-401	7.2	0.43	55	(48-60)
69-400			48	(33-58)
38-258	7.0	0.68	45	(18-65)
38-573	Used as monitor			
66-241	6.0	0.51	48	(27-60)
66-382			36	(1-48)
62-371	7.1	0.77	54	(25-72)
62-239			61	(19-76)
67-394	6.0	.48	34	(15-52)
67-227			23	(18-27)
60-384	6.0	.85	46	(27-62)
60-204	Monitor			
70-495	10.0	0.56	71	(45-115)
70-449			51	(22-64)
48-242	5.0	0.73	59	(40-69)
48-202			43	(26-49)
61-306	6.0	0.72	51	(35-58)
61-305			36	(15-50)

* From sheet resistance measurements on monitor P epitaxial substrates.

vity collector regions without very touchy compensation techniques which do not seem to be reproducible over a long time period. With new pure material better control of high-resistivity deposits should be achieved in the near future.

2.1.8 Summary

This section has discussed the theory behind epitaxial growth, problems encountered in the practice of this method, proposed methods of solving these problems, and the present process being employed in the prototype pilot line operation. Purity and resistivity control still stand out as the major problems to be solved. Thickness seems to be fairly well under control, as indicated by results of runs described on the prototype pilot line. Consideration is being given to methods of increasing the number of wafers deposited in a run. With the solution of these problems, the epitaxial process will be able to replace the present collector contact diffusion process, with reduction of labor and improvement of quality of the required transistors.

2.2 Base Predeposition and Redistribution

The present base predeposition process is a small batch operation which results in a high labor requirement. Since several predeposition runs are grouped together for a single redistribution, variations in the predeposition can result in control problems during the redistribution. Sheet resistance readings are taken on sample wafers after the predeposition, but the value after redistribution can not be reliably predicted from these readings. Better control could be achieved if both operations were performed on large lots of the same size. Ideally this would mean a single furnace operation with a simultaneous predeposition and diffusion. However, experiments indicate that this may be impractical since the predeposition must be accomplished at a temperature which is considerably below the diffusion temperature.

In order to increase the capacity of the predeposition, it is necessary to stand the wafers vertically in a slotted boat. The present method, which employs a boron oxide doped quartz flat as the source, can not be used conveniently in this configuration. However, a vapor deposition method of supplying the boron should be suitable provided that uniform coatings can be obtained on a large number of wafers at one time. This is expected to result in better control and a reduction of labor cost and furnace requirements.

It has been established that a vapor deposition method is desirable. This end could be accomplished by the oxidation and/or decomposition of any volatile boron compound. Since a uniform oxide coating can be obtained from the pyrolysis of ethyl silicate, the simultaneous decomposition of organic borates and silicates was attempted. Results indicate that these procedures are the most promising. Therefore, they have been under study during the past quarter. The boron-silicon ratio in the deposit may be controlled by any of several methods. These include

1. Premixing the silicate and borate compounds in the desired ratio.
2. Independent temperature control of each source to maintain their vapor pressures as required.
3. Dilution of the borate stream with an inert gas.
4. Use of a capillary to restrict the amount of borate vapor which enters the main flow of gas.

Initial tests were performed to determine the required silicon/boron ratio in the vapor. When the optimum ratio was obtained, it was found that the amount contained in the deposit could not be controlled by premixing the silicate and borate liquids. Therefore, the second method, maintaining the borate at a known temperature to limit its vapor pressure, was used. A cold trap filled with ice and water was employed to obtain a temperature of $0^{\circ}C$.

The base predeposition process is temperature-limited and an excess vapor concentration is used. This is followed by surface cleaning in hydrofluoric acid and by high temperature diffusion. The doped oxide predeposition occurs at a much lower temperature ($\sim 700^{\circ}C$); it is then used as a limited source for diffusion at a higher temperature. Some variation in surface concentration can be obtained deliberately by varying the ambient gas during this diffusion.

Several diffusion runs using this new process were made. The results can be summarized as follows:

1. The diffusion coefficient of boron from limited boron-oxide source is lower than the published boron diffusion values. The diffusion temperature had to be increased 20-25$^{\circ}C$ in order to obtain comparable depths in the same diffusion time.
2. Surface concentrations on the wafers from an individual predeposition run were very uniform, however, absolute values could not be duplicated reliably from run to run.
3. When successive predepositions were made, the boron concentration always decreased.

These results suggest that contamination in the predeposition furnace plays a major role in affecting the boron/silica ratio in the deposit. This effect could not be eliminated by cleaning the furnace tube and boat each time. Therefore, techniques

have been altered in order to add a known amount of deposit to the predeposition furnace each time. The furnace itself is then used as the boron source. This treatment is followed by deposition of an overlying undoped oxide followed by subsequent diffusion. Preliminary results indicate that good control and reproducibility are possible with this procedure.

Additional experiments must be run to determine the effects of tube doping time, predeposition time and oxide thickness. When the optimum operating conditions are found, larger batches of wafers will be run to determine the suitability of the process for use in the final production demonstration run.

The thermal decomposition of various boron compounds to be used as a limited source for base diffusion has been discussed. Deposition of a doped oxide film by pyrolysis of an organic borate and silicate is the most promising procedure being investigated. The overlaying of silica on the deposit results in a more uniform base predeposition.

This new method of predeposition is applicable to use on a large number of wafers standing in a slotted boat. After diffusion, the base surface concentration is found to be very uniform across any individual wafer, and there is little variation between wafers in any one run. With this improved control over the base diffusion operation, it is expected that the completed

transistors will exhibit more uniform electrical characteristics. An additional advantage expected is a material reduction in labor costs. Thermal erosion is also prevented during the diffusion run since the oxide layer forms a protective film on the silicon surface.

2.3 Emitter Diffusion

Following the base diffusion, the emitter pattern is etched in the oxide using standard photoresist techniques. The oxide which is grown during the base redistribution is sufficiently thick to mask the base areas during the emitter diffusion. It has been standard practice to vaporize phosphorus pentoxide and deposit it on the silicon wafers by using an inert carrier gas.

This procedure has several disadvantages. If any trace of water enters the system, the vapor pressure of the P_2O_5 will decrease and a low surface concentration will result. In addition, vapor droplets are carried through the furnace. If they deposit on the wafers, uneven junctions and penetration of the base mask may occur. Since excess P_2O_5 is used in this method the furnace tube soon becomes coated with a sticky phosphate glass mixture which must be removed following each run. This cleaning operation is time consuming. It would be desirable to generate only the required amount of P_2O_5 directly in the diffusion furnace. Such a process has been devised. It consists of the oxidation of the vapors of phosphorus exychloride. Other phosphorus com-

pounds have been tried without success.

Phosphorus oxychloride reacts with oxygen at elevated temperatures to form phosphorus pentoxide and chlorine. The chlorine which is evolved does not etch the silicon because of the oxidizing atmosphere. Several experimental runs were made to determine the optimum $O_2/POCl_3$ ratio and gas flow rate.

Results of several diffusion runs may be summarized as follows:

1. Surface concentrations and diffusion depths are comparable to those obtained with P_2O_5,
2. The phosphorus oxychloride must be maintained at a temperature near its freezing point (2^oC) to lower its vapor pressure so that P_2O_5 fumes are not seen at the exit end of the furnace. This results in a clean furnace tube.
3. There is reduced handling of the diffusant because the bubbler only needs to be refilled infrequently.
4. There is better control over the amount of P_2O_5 deposited on the wafers.
5. Since the P_2O_5 deposition is done in an oxidizing atmosphere, there is no apparent thermal etching of the exposed silicon.

The thermal decomposition of phosphorus exychloride in an oxidizing atmosphere results in a uniform phosphate glass coating

on the silicon wafers. There are no vapor droplets which can deposit on the slice and cause shorts through the base layer. The system is simpler to operate, requires less handling of the diffusant and chance of contamination particularly from water, and eliminates the need for cleaning the furnace tube after each run. The process should be feasible for automatic controls; these studies are in progress.

Diffusion runs on a large number of wafers will be made as soon as the required boats are fabricated. Only eight wafers can be run at once using the available equipment and standard inch and one quarter diameter wafers.

2.4 Photoresist Alignment

Photographic methods are employed in certain stages of our power transistor processing. Presently, photoresist masks are used in generating the precise geometry for the emitter diffused and the base and emitter metallized areas. Other possible uses for this method are to form the planar structure bases and to define mesa etching and dice etching geometry. Past development work has been quite successful. The remaining problems are improvement of quality, increased alignment accuracy, and reduced labor requirement through improved jigs and fixtures. A simultaneous increase in speed and accuracy of alignment appears possible by use of centerless ground silicon ingots with an aligning flat as base stock for manufacture. This should materially speed all jigging operations.

At present, alignment of the wafers to the film pattern is done by microscopic observation and by adjustment with one rotary and two translational micrometers which move the silicon wafer with respect to the photoresist photographic pattern. No problem is involved with the first photoresist process, but all subsequent photoresist operations must be aligned with the original masked area to a high degree of precision, preferably 0.1 to 0.2 mils. These subsequent alignments are quite time consuming, at the present time, and misalignment, especially with new operators, results in reject wafers. The proposed solution is to install three pins in the alignment jig. Two of the pins will rest against the flat side of the silicon wafer and the third pin will rest against the centerless ground edge,

thus precisely pre-positioning the wafers for all jigging operations. For Technical reasons, the flat should preferably be aligned with a crystallographic break plane in the wafer, so that dicing of the transistor modules from the wafers will be more reliable and less subject to rejects. It is anticipated that some "touch up" alignment will still be required due to etch damage and chipping of the alignment edges. However, the operation should be many times faster and more accurate, and gross misalignment should be rare.

A trial jig was made. To avoid damage to the photographic pattern, the alignment pins were installed to protrude above the wafer vacuum chuck slightly less than the wafer height. It was immediately discovered that wafer bowing and rounding of the wafer edges allowed the wafer to slide over the alignment pins without registering in a large number of wafers. Parallel lapped wafers which had not been diffused and etch polished could be properly aligned. Since the present process requires acid etching, the rounding of the edges cannot now be eliminated. Also, the bowing is a natural result of lapping and material removal from a wafer with a highly-doped collector contact region on one side and a high-resistivity collector region on the other. Even epitaxial wafers exhibit bowing when made as thin as is desired for the required transistors.

Two solutions are possible, elevating the pins above any normal bowing of the wafers and working with thicker material. In the former method the photographic patterns must be punched at the location of the alignment pins. The latter method requires subsequent removal of silicon from the back side of the wafer after all

photoresist alignment operations are completed to avoid an increase in thermal and electrical path in the collector contact region with resultant loss in device characteristics.

The extending of the pins seemed the easier solution. A new alignment jig part and a pattern punch have been designed and are to be constructed to test out this method. It is expected that this improvement will materially increase the speed and quality of the photoresist alignment operation.

2.5 Design of the Twenty-Ampere Transistor Structure

This program requires the development of a 20-ampere power transistor (type 3-20) as part of a family of interdigitated silicon NPN power transistors. While 20-ampere transistors were provided by Pacific Semiconductors, Inc. on the previous contract, AF33(600)-35088, the present program requires a device of higher collector voltage (100 V) and higher frequency response (25 megacycle operation at 10 db power gain). This is above the frequency capabilities of the previous device. In this section we will cover the design parameters believed necessary to meet the new specifications and report on progress during this quarter.

The voltage rating of the type of transistor to be made is largely determined by the electrical resistivity of the material making up the collector region. For reliable 100-volt operation, however, we must provide a margin of safety against damage by voltage surges and transients. A minimum V_{CEO} of 120 volts and a V_{CBO} of 160 volts should provide this safety margin. Design information would indicate

that the collector resistivity should exceed two ohm-centimeters. However, other considerations, such as surface and bulk leakage currents must be taken into account. Too high a resistivity must not be employed, however, to avoid excessive parasitic resistance, decreasing f_a, and space-charge-limited emission problems. Material of four to eight ohm-centimeters would be desirable; however, to increase usable yield per ingot, decrease wafer cost, and increase yield to the 100-volt specification, it appears advisable to employ 4 to 13 ohm-centimeter material.

The space charge width for the collector in the worst case, namely 160 volts and 13 ohm-centimeters resistivity material, can be found from the equation:

$$X_m = 3620 \frac{V_{max}}{N_c}$$

where X_m = space charge width in centimeters

V_{max} = 160 volts

N_c = carrier concentration of approximately 3×10^{14}

An allowance is also made for the depth of penetration of the base diffusion. The selected design target is 33 ± 4 microns.

For optimum heat dissipation the collector contact region should be as thin as possible. In the past, wafer thicknesses of 5.5 ± 0.5 mils have been found feasible. Use of thinner layers resulted in excessive breakage during processing, especially when the large 1.25 inch diameter wafers are employed. Experiments have been conducted with 3.4 ± 0.4 mil wafers. It is now believed feasible to handle these wafers with appropriate jigging and use of vacuum

pick-up tools; however, wafer bowing is then found to be a serious problem. A possible solution is to employ thicker wafers during processing and remove the excess material by lapping or etching just before completion of the dicing of individual transistors from the completed wafers. This will enable the desired wafer thickness to be achieved, but entails an additional processing step. In the event this procedure is impractical, the original wafer thickness of 5.5 ± 0.5 will be necessary instead of the more optimum 3.4 ± 0.4 mil dimension.

The required 3-20 type transistors must dissipate 180 watts in order to have a power output of 120 watts at 25 megacycles and 40% collector efficiency as called for in the device specifications. Thermal resistance calculations indicate that a copper heat transfer surface placed in contact with a well-cooled heat sink should have a diameter of 1-1/16" or greater to avoid excessive temperature rise in the device. The use of copper for the stud and heat sink materials appears to be most advantageous to reduce device to heat sink thermal drop. Aluminum does not appear satisfactory due to the higher thermal resistance. With a cooling fin temperature of $50^{\circ}C$ the fin-to-stud temperature rise at 180 watts is expected to be $54^{\circ}C$ for commercial tolerance surfaces and the internal stud-to-silicon hot spot temperature rise is estimated to be $46^{\circ}C$ for a junction operating temperature of $150^{\circ}C$. The junction structure will be described later in this section.

For the required 25 megacycle operating frequency, a design calculation has been made based on high-frequency design theory. A con-

venient and powerful tool for the analysis of transistor design is the power gain band width squared figure of merit. The derivation of new frequency design equations is beyond the intended scope of this development program. However, detailed derivations and discussions are to be found in the literature, for example, the work of J. M. Early.[12] By proper analysis of the equivalent circuit, it can be shown that the frequency response is related to the emitter stripe width and the base thickness under the active emitter region, while the current handling capability depends mainly on the effective emitter-base edge length.

It was determined by the above type of analysis that suitable frequency response could be obtained by utilizing an eight-mil wide emitter stripe and an effective base thickness of one micron. For a 20-ampere current-carrying capacity an emitter base edge length of 5.0 inches is required. The pattern chosen is of the interdigitated or "comb" type and has 22 emitter fingers of 8 by 112 mil dimension. The pattern is divided into two "mirror image" halves for purposes of fitting a square transistor module shape and for better distribution of heat generation over the wafers. Appropriate "comb backs" have been provided for lead attachment of the emitter and the base leads. The structure is believed to be a considerable improvement over the pattern employed during the previous work on Contract AF 33(600)-35088, but the structure remains to be tested.

Other device parameters are determined by the need for a high emitter efficiency and current gain requirements. An emitter sheet resistance of three to four ohms per square, an emitter depth of approximately

two microns, a total base depth of approximately three microns, and a base sheet resistance of 180 ohms per square are considered good design objectives based on past experience. The required transistor master patterns for the type 3-20 transistor have been designed and are under construction. When completed, sample transistors will be made to prove the feasibility of the design. Testing at high frequency under full power will necessitate completion of an adequate mounting and lead attachment. The mounting development work will be covered later in the report.

The lead size is determined by current-carrying capabilities. At present the preferred metal is silver, although molybdenum, copper, gold, or aluminum could conceivably be employed. The minimum emitter lead size is No. 20 gauge (0.032" diameter) silver wire. The two base leads should be of No. 24 gauge (0.020" diameter) silver, each. Other materials should have additional cross sections to compensate for higher heat generation at high current and lowered fusing rating of the material. The exact lead configuration will require analysis of high-frequency performance and will require additional wor.

In this section we have discussed the design of the 3-20 type transistor. Most of the critical design parameters have been chosen, but testing of actual transistors will be required to prove the adequacy of the design. Patterns are currently being made so that samples can be produced for actual operational tests.

CHAPTER 3

Package Engineering

The principal effort of the package engineering group during this quarter, has been directed toward the design and procurement of package prototypes.

The first generation of the 1 ampere transistor will utilize a conventional TO-8 resistance welded package until a cold-welded copper body version is design proven.

Samples of a double-ended cold-welded package for the 10 and 20 ampere transistors are on order. The stud and cap of the package are formed by cold extrusion of O.F.H.C. copper, a method which assures close dimensional tolerances and excellent mechanical and thermal properties.

Samples of a hex O.F.H.C. copper stud have been received, and will be evaluated for the air cooled versions of the 50 and 100 ampere transistors.

Design work has not been completed on the 50 to 100 ampere liquid cooled transistors, but preliminary work indicates that a coaxial package comprised of O.F.H.C. copper rings and flanges, insulated with ceramic rings, and a copper cap which would be cold-welded, is feasible.

CHAPTER 4

Conclusions

In this report we have discussed problems to be studied during the improvement of manufacturing processes for the family of transistors required by this contract. The substitution of an epitaxial collector process for the present collector contact diffusion process appears advisable both to improve device electrical characteristics and manufacturability. Some theoretical considerations in epitaxy have been covered. Principles such as the apparent necessity to maintain supersaturation of silicon atoms in the vicinity of the growing surface layer have been discussed. The choice of trichlorosilane as a source material is based on ease of decomposition in a hydrogen stream and practical considerations, such as temperature of deposition and availability in adequate purity.

To obtain collector regions of the correct resistivity for the desired devices, silicon layers of approximately eight ohm-centimeters are desired. The problem of purification of trichlorosilane to meet these requirements has been studied and progress has been made. Various techniques studied to improve processing and equipment improvements for better pilot operation are described. Three approaches to resistivity control were outlined and progress to date has been given. The preparation of wafers for epitaxial deposition is briefly considered. The work on epitaxy must lead to the construction of a prototype pilot plant capable of running a large number of wafers at a time. A brief

description of the operation and results has been included. Since resistivity control problems have not been completely solved, trial runs had to be made for lower resistivity than is required for the finished devices. However, valuable operating experience was obtained which should shorten the lead time for application of the method to the required transistors. Process control charts indicate stable operation can be achieved both in regard to collector thickness and resistivity.

Work on a vapor deposition method of producing a boron-silica base predeposition have been quite successful. A large scale run will be required to determine if problems of control and uniformity result when a large number of wafers are treated in a batch. No significant problem in redistribution of the vapor deposited base material has arisen and additional work on base redistribution diffusion is not required at this time. The use of phosphorus oxychloride and oxygen in place of phosphorus pentoxide has also shown promise during smaller emitter diffusion trial runs. Large scale tests will be required.

An attempt to improve the photoresist alignment speed and accuracy by use of guide pins in the wafer jig was unsuccessful due to wafer bowing and rounding of wafer edges. An altered jig with pins extending through punched holes in the photoresist pattern is expected to overcome this difficulty.

The design for the 20-ampere transistor (type 3-20) was completed. Process parameters have been determined. Samples will be made to test the suitability of the design as soon as master patterns are completed.

Package design studies have been started. An attempt will be made to limit the number of packages to four. Parts and equipment have been ordered for the development of cold weld techniques for the package sealing operations.

CHAPTER 5

Program For The Next Period

Process development work during the coming quarter will, in general, continue the projects now in operation. In addition, it is expected that new development work on the problems of wafer etching to a precise thickness and an improved mounting method will be undertaken.

In the epitaxial collector process development, the major emphasis will be on obtaining resistivity control in the 8 ohm-centimeter range. Work will continue on improved manufacturing techniques and processes and on purification of the trichlorosilane. Some work on the propagation of dislocations during epitaxial growth may be required pending the outcome of current wafer evaluation studies. A high degree of material perfection is believed necessary for the 4-50 and 5-100 transistor types.

Large scale tests of the new boron-oxide base predeposition process will be required to prove its suitability as a manufacturing method. It must be determined how large a batch size can be used without adverse effects on process control and base-layer thickness and resistivity uniformity. At present, the base redistribution process is satisfactory. However, the new base prediposition process will require that tests be made at least through redistribution for evaluation purposes.

The new phosphorus oxychloride and oxygen emitter diffusion process will also require large scale testing. Resistivity and angle lap

evaluation will be employed for preliminary evaluation, but some finished transistors will be produced to prove the suitability of the method.

It is planned to complete a special vacuum chuck to hold wafers during acid etching. This should enable the elimination of the present wax mounting method. Wax mounting, demounting, and cleaning requires excessive labor, and wax residues are deleterious if not removed.

The building and testing of the improved photoresist alignment jigging should be completed during the next quarter. If satisfactory, improved jigging and necessary process changes will be applied to the pilot line.

The patterns for the 3-20 type transistor will be completed during the coming quarter, and samples will be made for evaluation. Work will begin on design of the 4-50 and 5-100 types. The results of tests on the 3-20 will be employed to guide the design of the 2-10 type, and a final pattern and device parameter selection may be possible for both the 2-10 and 3-20 by the end of the period. The final design of the 4-50 and 5-100 types must await the evaluation of preliminary transistors of these large sizes.

Development work on improved transistor mounting "solders" are scheduled to begin early in the coming quarter. A target of a solder melting above 300°C has been set to improve device reliability under 200°C storage. It is believed that the softening point of the present solder is too close to the 200°C storage temperature requirement for an adequate margin of safety.

Various package prototypes which are now on order will be received and evaluated as to their suitability. Development of cold sealing tooling and techniques will be carried out during the next period.

ILLUSTRATIONS

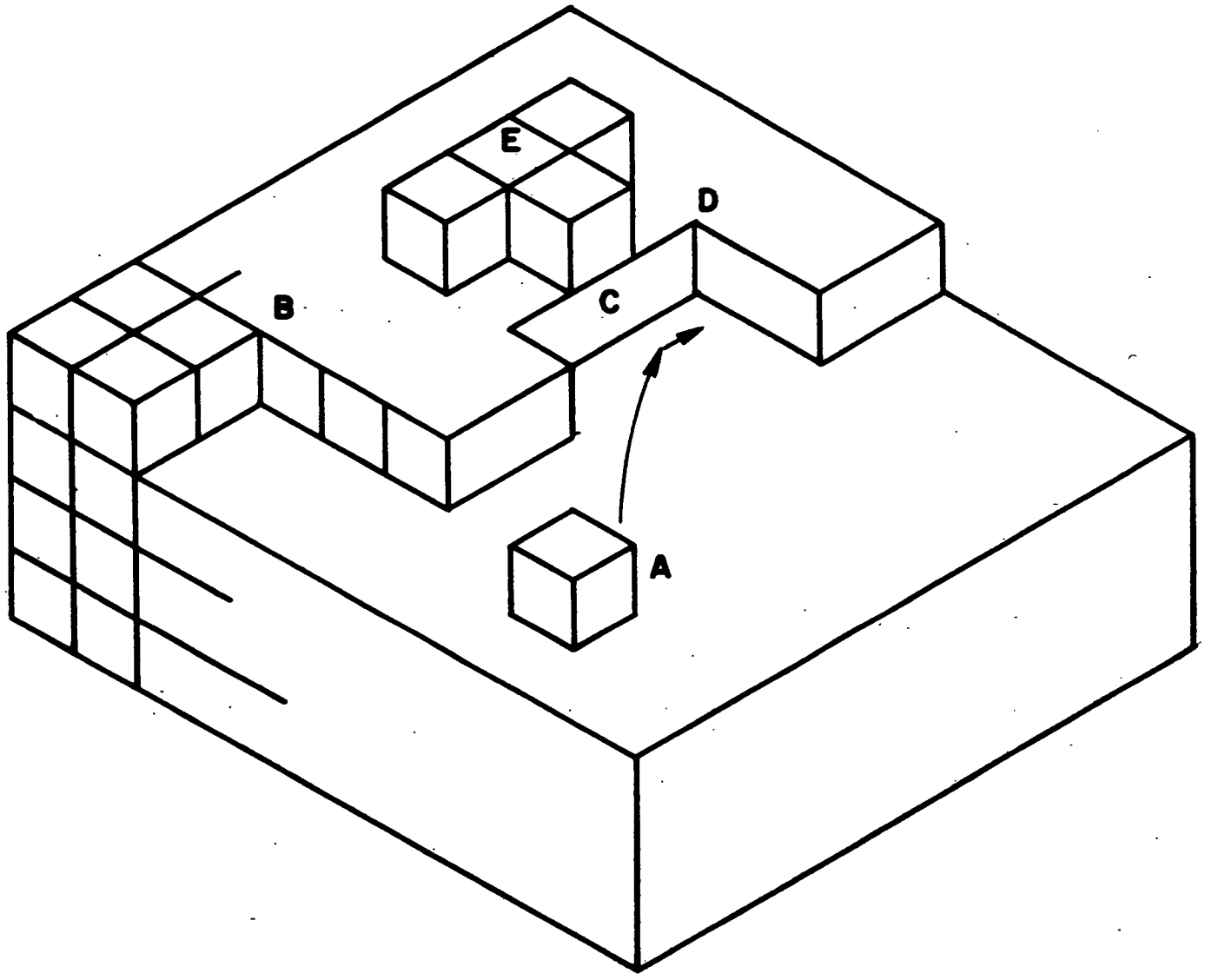

Fig 1 KOSSEL CUBE MODEL

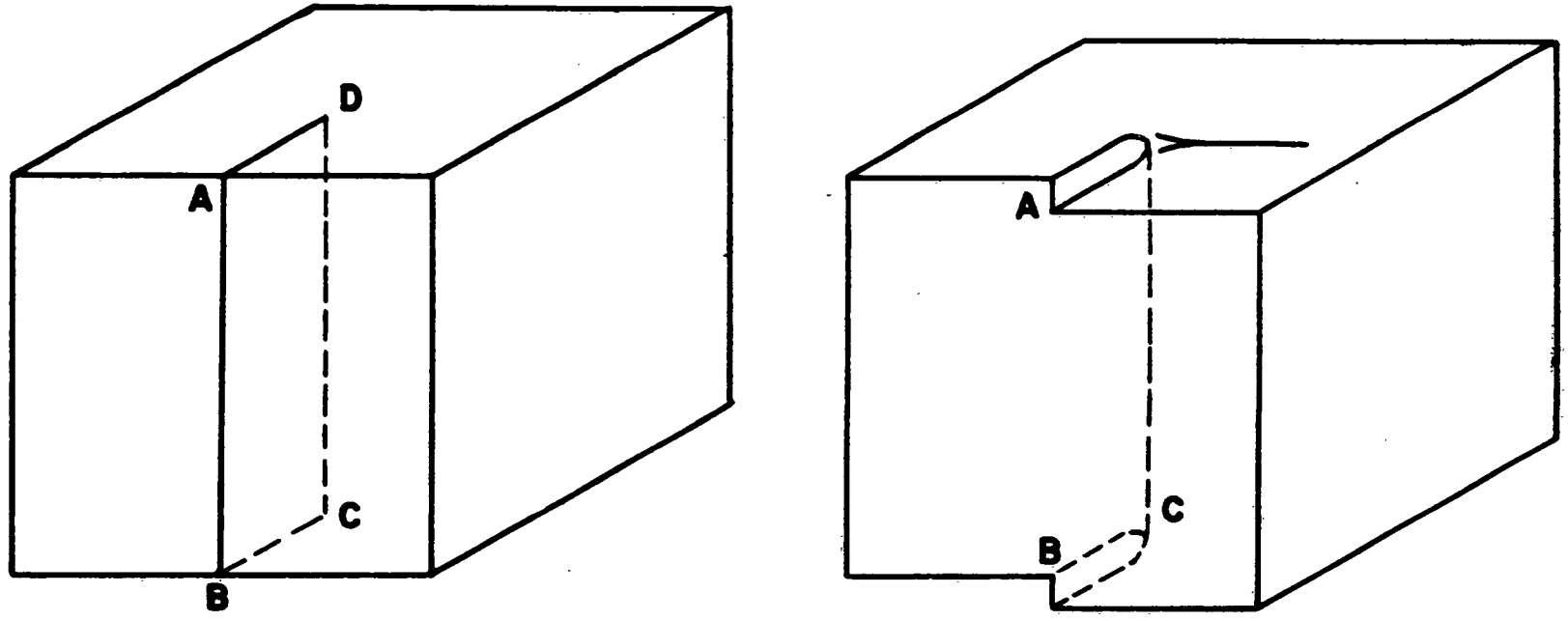

Fig.2 FORMATION OF SCREW DISLOCATION

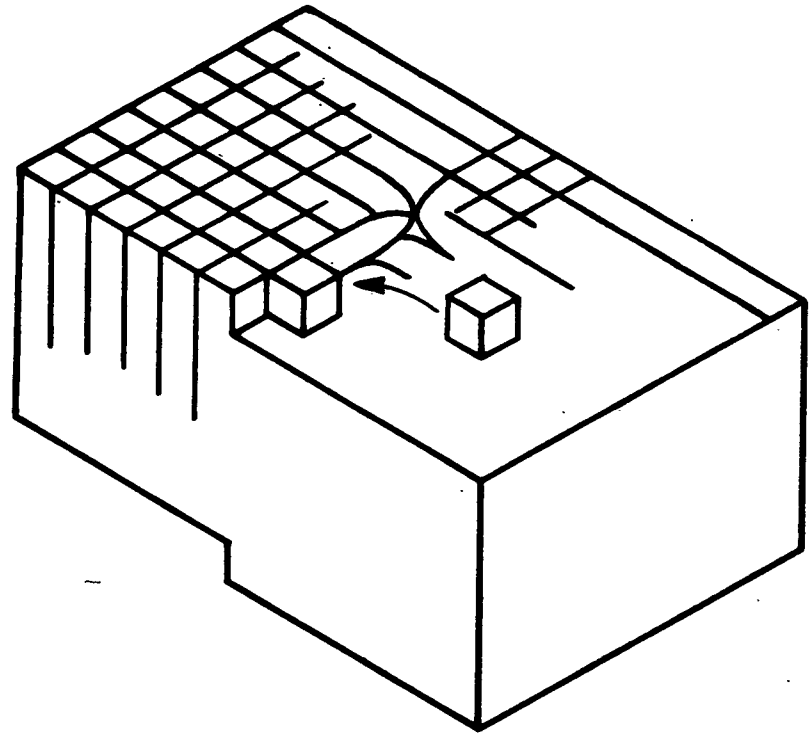

Fig.3 SCREW DISLOCATION NORMAL TO UPPER SURFACE

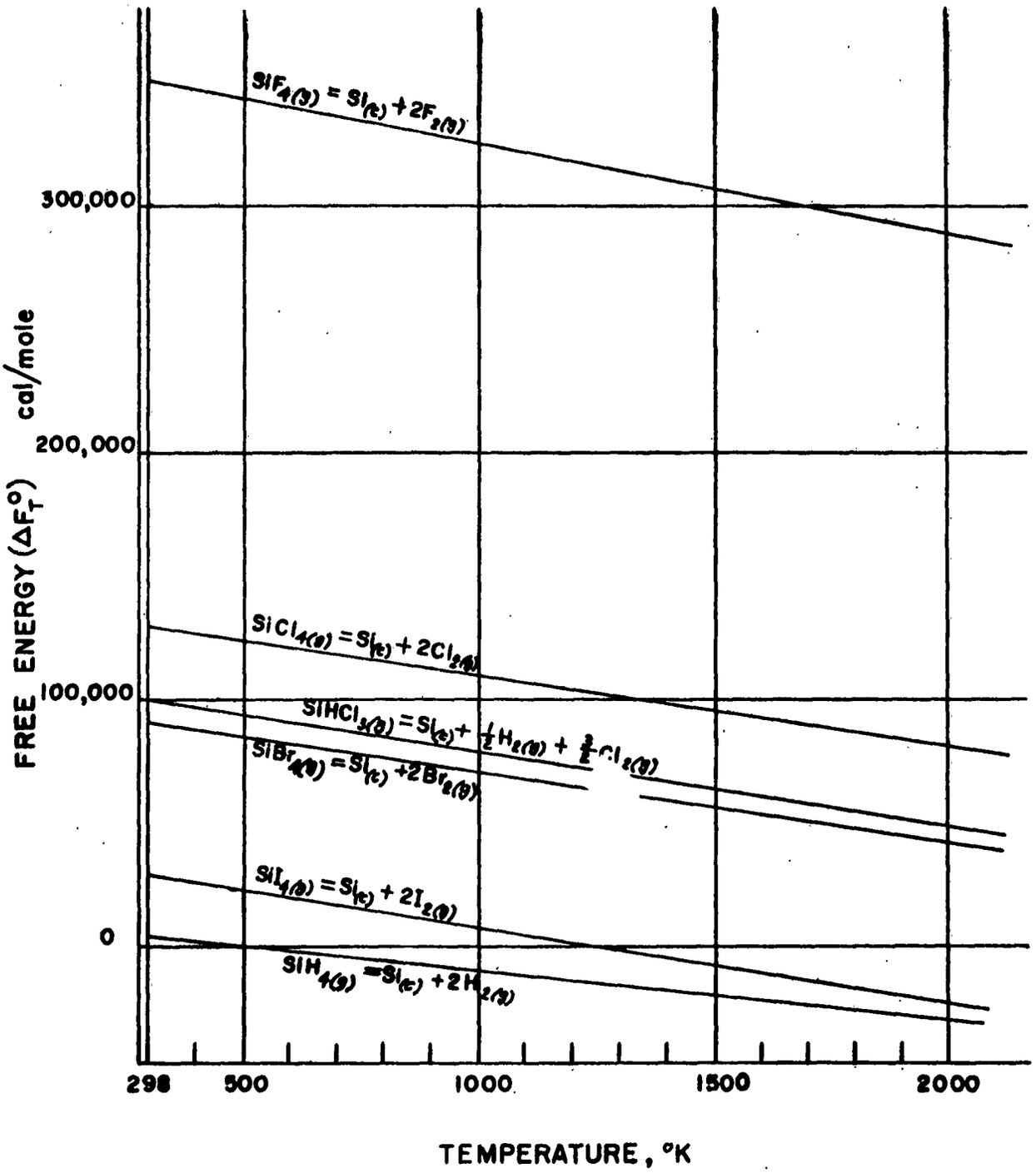

FIGURE 4 FREE ENERGY—TEMPERATURE CURVES FOR SILANE, SILICON TETRAHALIDES AND TRICHLOROSILANE

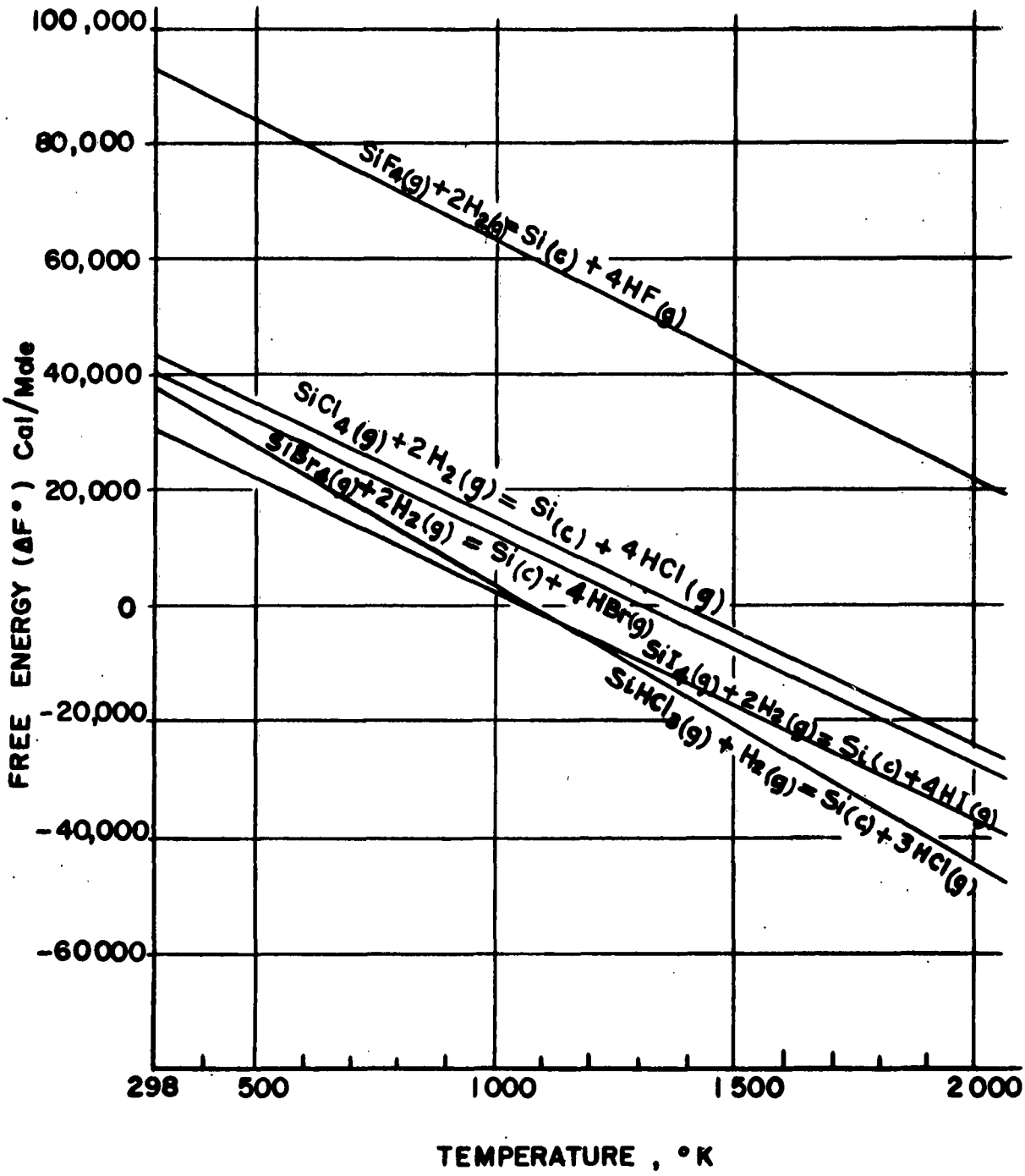

FIGURE 5 FREE ENERGY TEMPERATURE CURVES FOR SILANE SILICON TETRAHALIDE AND TRICHLOROSILANE IN THE PRESENCE OF HYDROGEN.

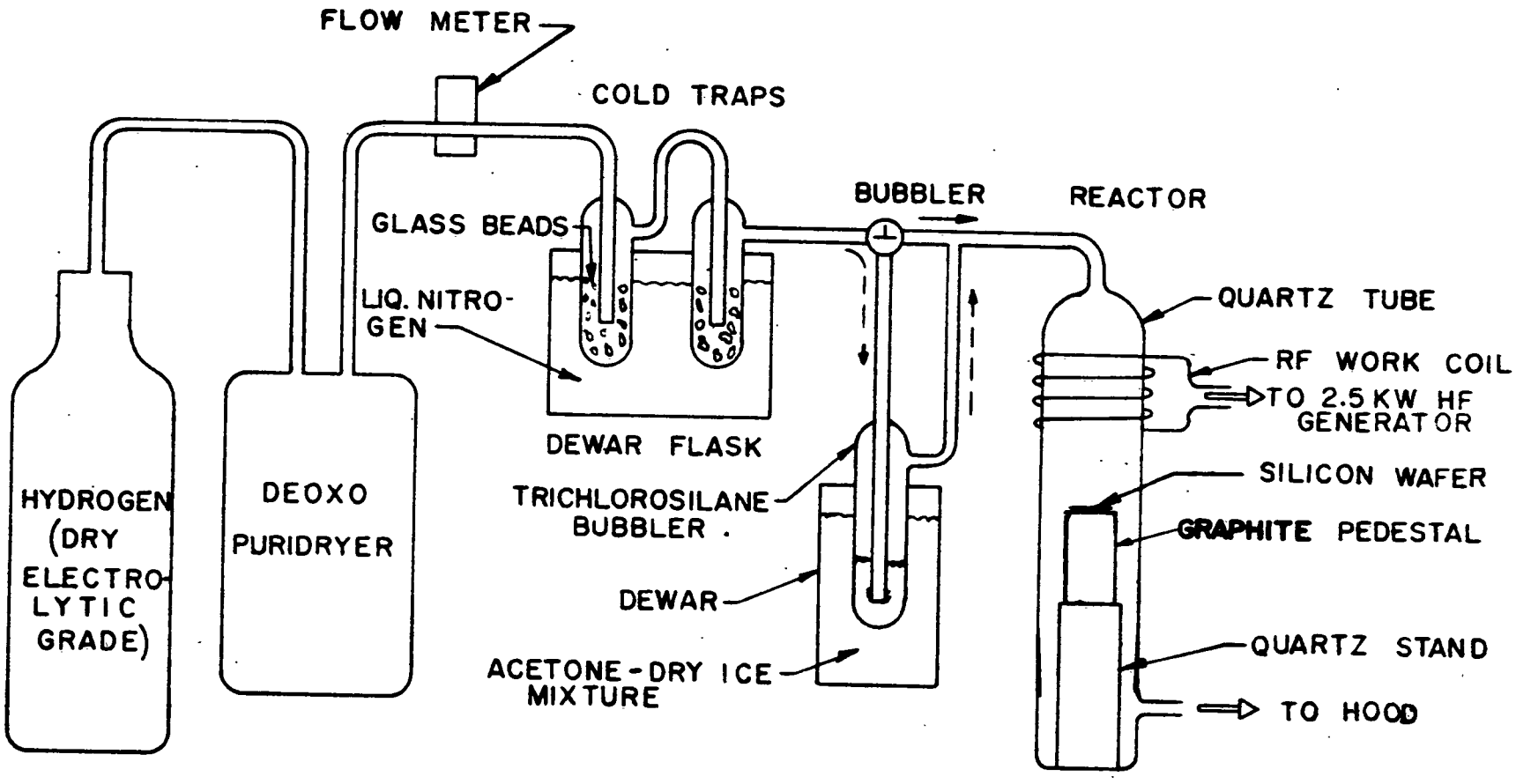

FIG. 6 SCHEMATIC OF HYDROGEN PURIFICATION SYSTEM AND VAPOR DEPOSITION EQUIPMENT

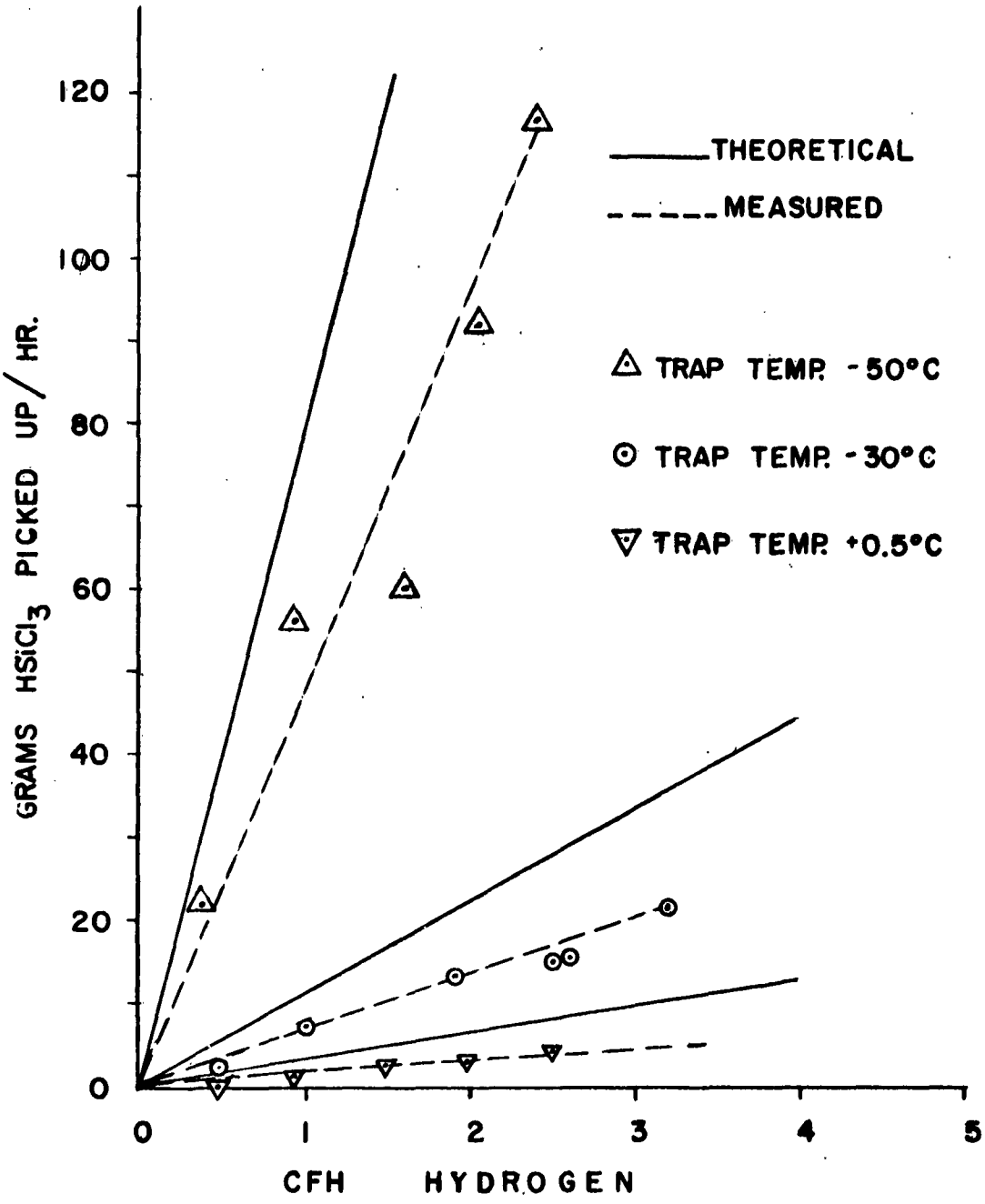

FIG. 7 TRICHLOROSILANE PICKUP vs. HYDROGEN FLOW RATE FOR BUBBLER TRAP PICKUP SYSTEM

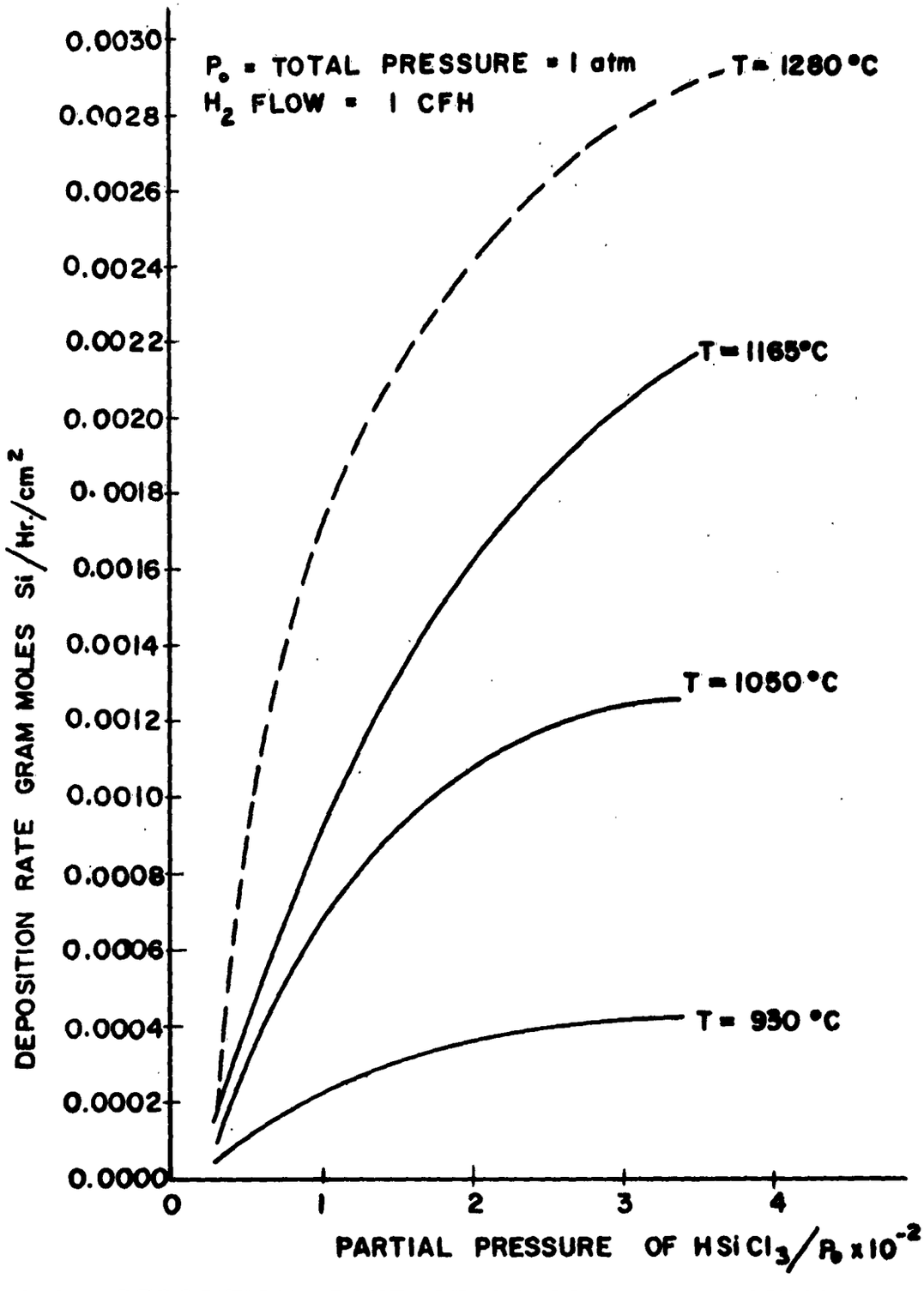

FIG. 8 DEPOSITION RATE OF SILICON VS. PARTIAL PRESSURE OF TRICHLOROSILANE

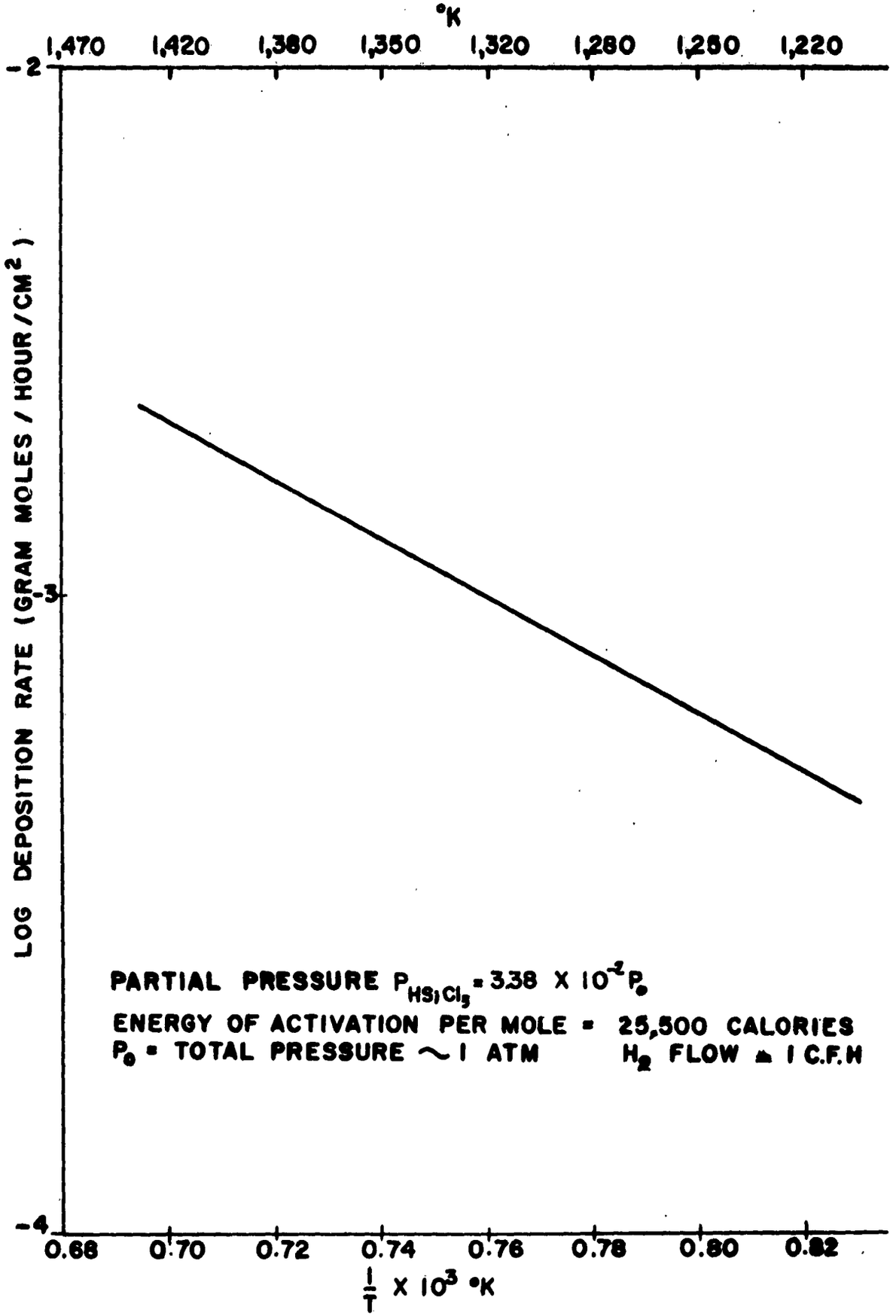

FIG.9 DEPOSITION RATE OF SILICON VS. TEMPERATURE

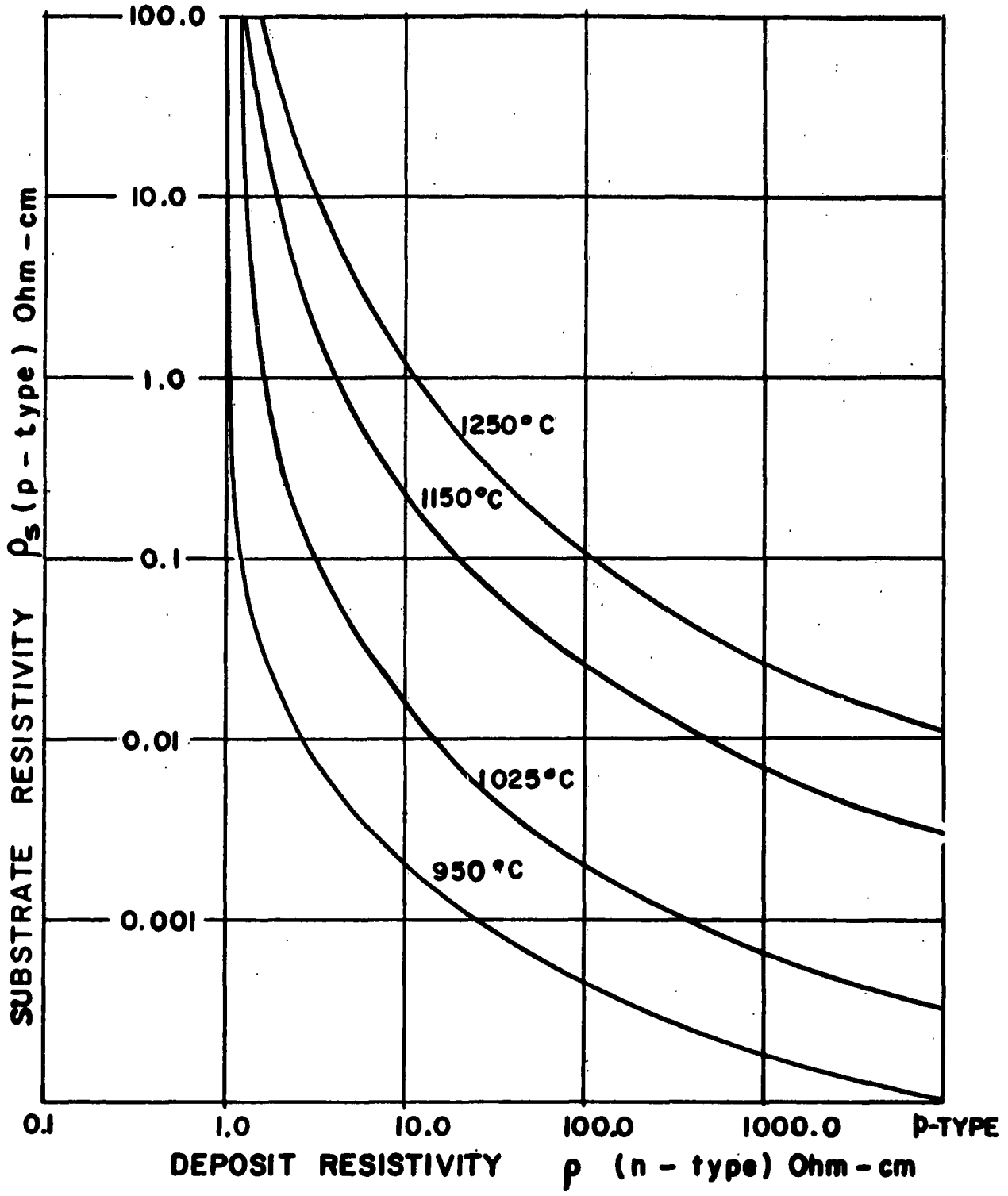

Fig. 10 DEPOSITION DATA

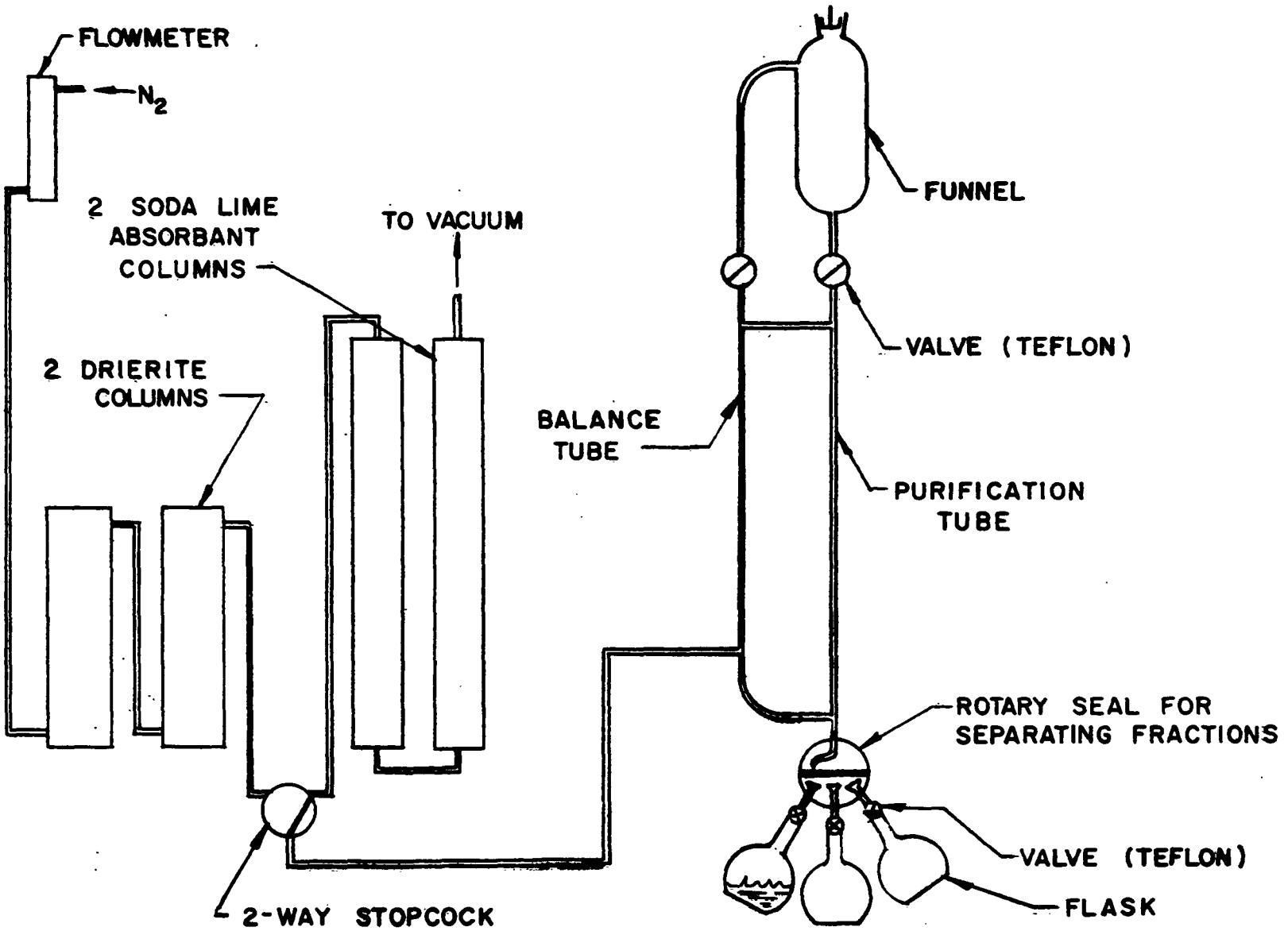

FIG. 11 TRICHLOROSILANE PURIFICATION APPARATUS

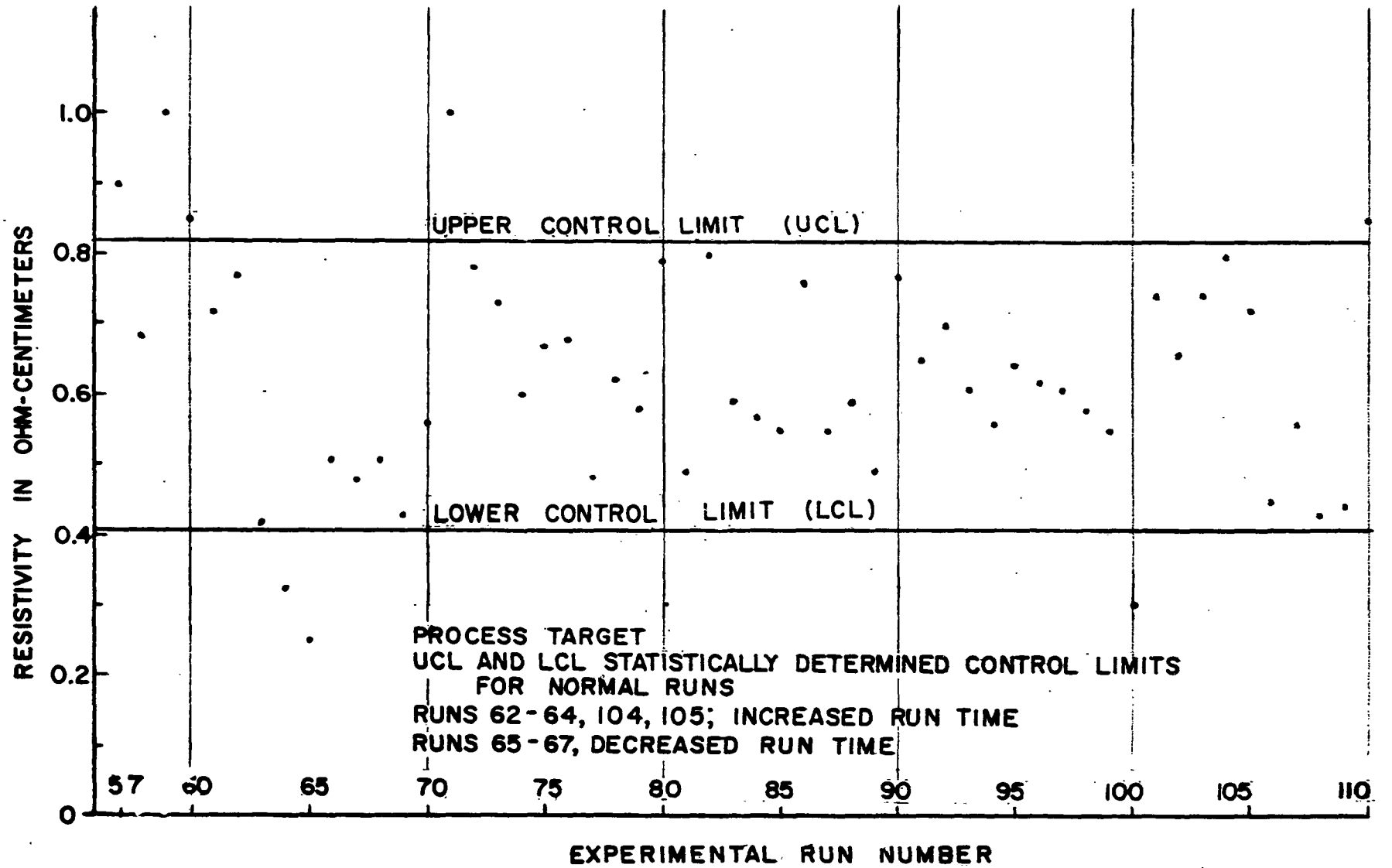

FIG. 12 RESISTIVITY OF EPITAXIAL COLLECTOR ON EXPERIMENTAL RUNS

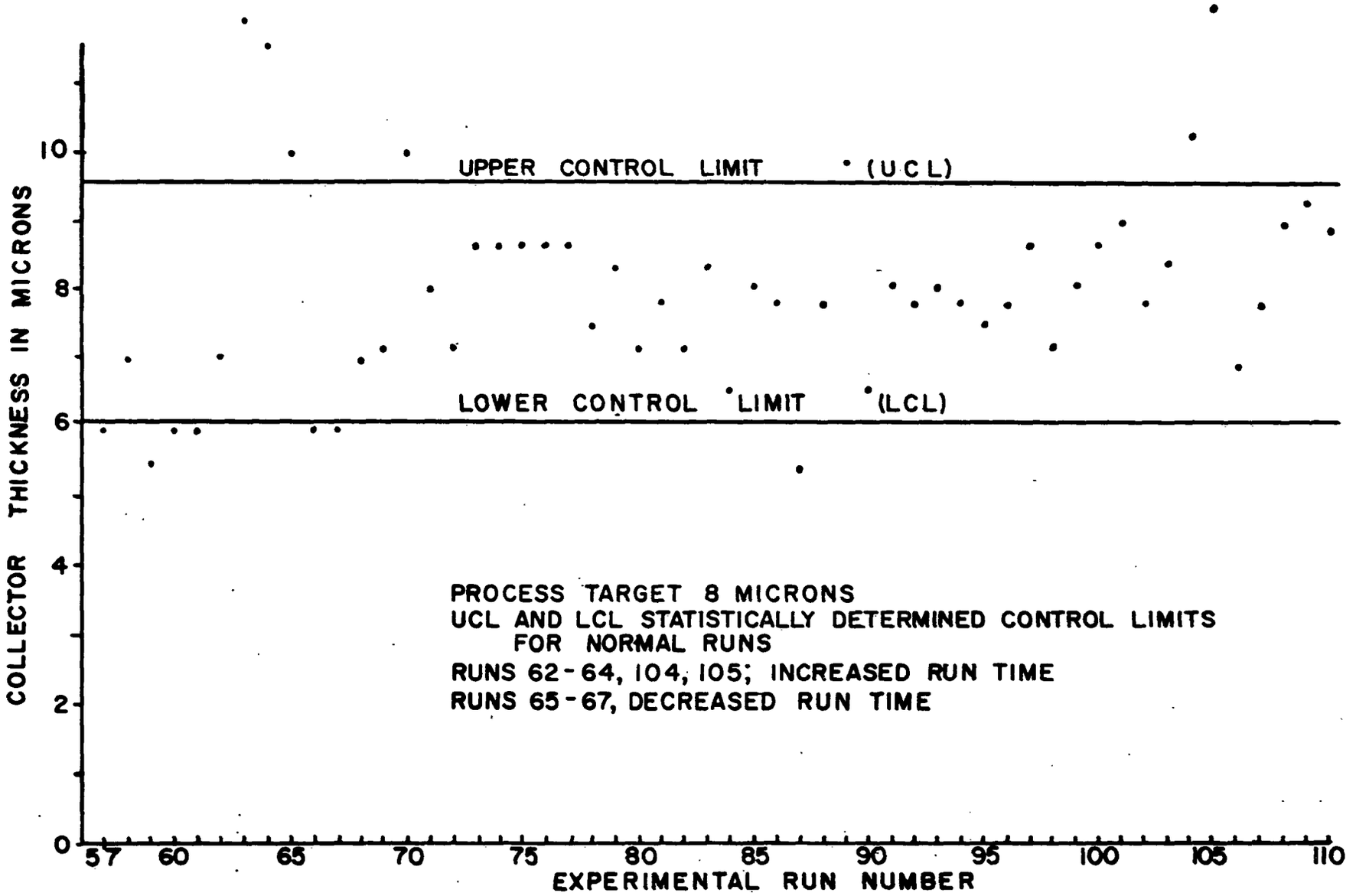

FIG. 13 THICKNESS OF EPITAXIAL COLLECTOR ON EXPERIMENTAL RUNS

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(Contract AF33(600)-43029) Unclassified report

The development of manufacturing methods and processes for the production of a line of "comb" structure silicon power transistors is discussed. Analysis of the sequence of operations indicate the desirability of investigating a planar design using epitaxial techniques for collector deposition. Problems of doping and resistivity uniformity require extensive study. Diffusion, etching and assembly operations were studied with a view to improving fabrication techniques. Twenty ampere transistor design parameters are described.

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